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InSb Charge Coupled Infrared Imaging Device - 20-Element Linear Imager

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J. D. Langan, and S. C. Chase

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Prepared for
Langley Research Center
under Contract NAS1-14922

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SYMBOLS

γ	=	parallel edge inefficiency parameter
ϵ	=	inefficiency per transfer of CCD
ϵ_o	=	free space permittivity, 8.854×10^{-14} f/cm
ϵ_s	=	substrate permittivity, f/cm
ϵ_{ss}	=	inefficiency due to surface states
λ	=	wavelength, μm
$\tau(\lambda)$	=	transmission of spectral filter at wavelength λ
τ_g	=	generation lifetime in depletion region, seconds
ϕ_{MS}	=	metal-semiconductor work function difference, volts
ϕ_s	=	surface potential, volts
Ω	=	field-of-view (FOV), degrees
A_{aper}	=	blackbody source aperture area, cm^2
A_B	=	CCD bit area, cm^2
A_D	=	detector area, cm^2
A_{DK}	=	area contributing to dark current, cm^2
A_E	=	channel edge area, cm^2
A_{FZ}	=	area swept by fat zero charge, cm^2
A_G	=	gate area, cm^2
A_J	=	junction area, cm^2
A_S	=	total area swept by charge packet, cm^2
A_t	=	trap area, cm^2
A_v	=	voltage gain
BV	=	junction breakdown voltage, volts
C_{CSM}	=	output diode to channel stop metal capacitance, farads
C_{FB}	=	flatband capacitance per unit area, f/cm^2
C_{gs}	=	gate-to-source capacitance, farads
C_{IDL}	=	ideal capacitance of MOS capacitor, farads
C_o	=	CCD output capacitance, farads
C_{OD}	=	output diode capacitance, farads

C_{OX}	=	oxide capacitance per unit area, f/cm^2
C_{PAD}	=	pad capacitance, farads
C_{SF}	=	source-follower input capacitance, farads
C_{stray}	=	stray capacitance, farads
CTE	=	charge transfer efficiency (efficiency per transfer)
$\bar{d}$	=	mean diameter of trap, cm
D	=	distance from blackbody aperture to device, cm
D^*	=	detectivity, cm $Hz^{\frac{1}{2}}$/watt
E_B	=	field in bulk depletion region, volts/cm
E_g	=	bandgap, eV (joule)*
E_s	=	surface electric field, volts/cm
E_y	=	lateral electric field magnitude, volts/cm
f_c	=	CCD clock frequency, Hz
F_{sc}	=	electric field in tunneling calculation, (volts/m)
$\hbar$	=	reduced Planck's Constant, 1.0554×10^{-34} joule second
H_{sig}	=	signal irradiance at plane of array, watts/cm^2
I_R	=	junction reverse current, amp
I_{sc}	=	photodiode short-circuit current, amp
J_D	=	dark current density, amps/cm^2
J_g	=	thermal generation current, amps/cm^2
J_T	=	current density due to interband tunneling, amps/cm^2 (amps/m^2)
k	=	Boltzmann's Constant, 1.38×10^{-23} joule/K
K_{OX}	=	oxide dielectric constant
L	=	CCD gate length, cm
m^*_i	=	effective mass, i = x,y,z, (kg)
n	=	number of transfers
N	=	number of detectors in TDI
N_B	=	number of CCD bits

*The interband tunneling calculations in Section 2 are facilitated through use of mks units, which are listed in parentheses in the list of symbols.

N_D = substrate net impurity concentration, cm^{-3}

N_{fc} = number of oxide charges per unit area = Q_{fc}/q, cm^{-2}

N_G = number of gates in CCD

n_i = intrinsic carrier concentration, cm^{-3}

n_s = surface electron concentration, cm^{-3}

N_{ss} = surface state density, $\#/cm^2\text{-}eV$

p = number of CCD phases

P = interband matrix element, (joule-meter)

q = electron charge, 1.6×10^{-19} coulombs

$Q_\lambda(T)$ = spectral radiant photon emittance of blackbody at temperature T, phot sec^{-1} cm^{-2} μm^{-1}

Q_B = background photon flux at plane of array, phot/sec-cm^2

$Q_{bb}(T)$ = radiant photon emittance of blackbody at temperature T, phot/sec-cm^2

Q_D = dark charge, coulombs

Q_{fc} = oxide fixed charge density, coulombs/cm^2

$Q_{FILT}(T)$ = radiant photon emittance of blackbody at temperature T transmitted by a specified filter, phot/sec-cm^2

Q_{FZ} = fat zero charge, coulombs

Q_p = stored charge density, coulombs/cm^2

Q_s = signal charge, coulombs

Q_{sig} = signal irradiance at plane of array, phot/sec-cm^2

Q_{trap} = trapped charge, coulombs

R_λ = responsivity at wavelength λ, volts/watt

T = temperature, degrees Kelvin

T_C = CCD clock period, seconds

T_{INT} = detector integration time, seconds

t_{OX} = oxide thickness, cm

T_S = storage time, seconds

V_{BI} = junction built-in voltage, volts

V_{FB} = flatband voltage, volts

V_{FT} = feedthrough voltage at output, volts

V_{FZ} = output voltage due to fat zero charge, volts

V_G = gate voltage, volts

V_n = noise voltage, volts

V_o = $V_s + V_{FZ}$, total output voltage, volts

V_R = junction reverse bias, volts

V_s = output voltage due to signal charge, volts

w = CCD gate width, cm

W = depletion region width, cm

$W_\lambda(T)$ = spectral radiant emittance of blackbody at temperature T, watts $cm^{-2}\ \mu m^{-1}$

$W_{bb}(T)$ = radiant emittance of blackbody at temperature T, watts/cm^2

$W_{FILT}(T)$ = radiant emittance of blackbody at temperature T transmitted by a specified filter, watts/cm^2

Section 1

INTRODUCTION

For new generations of infrared sensors in the 1980s, the development of integrated focal plane arrays (FPAs) will allow considerable improvements in sensor performance while reducing the weight, volume, and power requirements of the FPA and associated subsystems. An optimal type of integrated FPA is a charge-coupled infrared imaging device, or CCIRID, which combines, monolithically, detector elements and charge transfer devices for multiplexing or other signal processing functions in a common, infrared semiconductor material. Such CCIRIDs may be configured in either linear or area (two-dimensional) arrays.

Monolithic integration of detectors and CCDs in an intrinsic IR semiconductor material is an attractive approach for next-generation line and area IR arrays. The monolithic intrinsic structure offers higher operating temperature and quantum efficiency compared to its monolithic extrinsic (Si:X) counterpart having the same cutoff wavelength, but gains these advantages without the need for the hundreds or thousands of individual interconnections required in the hybrid IR array concept, a sandwich of an intrinsic detector array and silicon CCD chip. Because the intrinsic or fundamental absorption is utilized, potentially high quantum efficiencies may be realized with suitable device design, and optical crosstalk effects, particularly important in dense arrays, will be small.

The long range objective of this work is to develop this new concept in monolithic infrared imaging. The semiconductor material used in this development is indium antimonide (InSb), an excellent choice for a CCIRID with photon detection capability in the 1- to 5.5-μm spectral region. The immediate goal is to fabricate prototype InSb CCIRIDs that will be used to establish applications and operational characteristics of the infrared imaging sensors. The monolithic infrared CCIRID imagers being developed on this program are

intended for potential applications such as: sensors for earth resources management, for example agricultural, geological resources, and coastal zone monitoring; meteorological observations from space, such as temperature sounding; IR astronomy; and various strategic sensor applications. In some of these, the design of the chip for TDI of the detector signals in the CCD to enhance signal-to-noise ratio is desirable, and the technology being developed is ideal for such arrays.

The feasibility of InSb CCIRIDs has been demonstrated through achievement of a series of InSb CCD devices and basic InSb metal-oxide-semiconductor (MOS) measurements in previous NASA development contracts. An important milestone was achieved under contract NAS1-13163 with the first successful fabrication and demonstration of charge transfer in an InSb CCD[1]. The relatively low charge transfer efficiency (CTE) of these first devices (0.90), due to limitations in achievable gate dimensions at that time, was improved by dimensional reductions in a second chip design to 0.975[2]. The present CCIRID chip, the 8585 chip, which utilizes a totally new fabrication process as well as reduced dimensions, has improved CTE yet again to 0.995 in measurements to date, and should result in CTEs up to 0.9999 as the characteristics of the SiO_2 gate oxide are continually improved. The improved fabrication process, which eliminates the limitations inherent with the earlier techniques, includes planar junction formation and an aluminum and SiO_2 material system which is amenable to state-of-the-art chemical and plasma delineation techniques. Further, the new chip successfully integrates, for the first time in monolithic format, InSb IR detectors with an InSb CCD.

This report describes the design and fabrication of the 8585 InSb CCIRID chip, the principal device on which is a 20-element linear imaging device, and the electrical and optical characteristics of the experimental devices that were determined under this contract. The report is organized as follows. Section 2 describes the device design and fabrication, including discussion of the InSb material characteristics, the design and description of the 8585 chip, the fabrication process, and mask and process modifications that were implemented

in the program. In Section 3, test results for the two-element InSb CCIRID on the 8585 chip are discussed, which was the first device produced with the new process successfully operated. Included are: evaluation of the gate oxide characteristics; development of the surface potential diagram; discussion of the CCIRID channel stopping approach; and operation of the two-element device. Section 4 gives a similar discussion of test results for the 20-element CCIRID, including gate oxide characteristics, test equipment configuration, measurement of CTE, and optical mode operation. Section 5, Discussion of Test Results, examines some of the factors that have been identified which influence the current performance of these arrays, along with means of improvement. Section 6 describes part of a continuing survey of future instruments and sensor systems in which potential applications exist for the monolithic InSb CCIRID technology that is being developed. Finally, Section 7 summarizes the achievements of this contract.

Identification of commercial products in this report is to adequately describe the materials and does not constitute official endorsement, expressed or implied, of such products or manufacturers by the National Aeronautics and Space Administration.

Section 2

DEVICE DESIGN AND FABRICATION

InSb MATERIAL CHARACTERISTICS

InSb Wafers

Starting material for CCIRID processing was n-type InSb grown by M. C. P. Electronics Limited (England) and distributed by Metal Specialties, Inc., Fairfield, Connecticut. The InSb ingots, grown by the Czochralski technique, were cut into wafers oriented to within $\frac{1}{2}^{\circ}$ of the (111) plane, and subsequently final-polished to a thickness of 635 μm. The (111) B face was used throughout this program for device processing. The wafers used for CCIRID processing were undoped (n-type) with a net carrier concentration at 77 K ranging from 6×10^{13} to $2 \times 10^{14}/cm^3$, as determined by Hall measurements. The wafers utilized during the program had dislocation densities (as measured by etch pit density on the A face) ranging from 0 to $1000/cm^2$. Later in the program the E. P. D. specification was tightened to $\leq 100/cm^2$.

The wafers were shaped (by M. C. P.) to a uniform diameter of 3.2 cm, followed by cutting of a nonoriented flat. The uniform diameter and flat allow the slices to be handled conveniently in conventional processing equipment and are necessary for pattern orientation in the projection mask aligner that is used. An ultrasonic cutting tool was first used to shape the InSb wafers, but edge chipping led to the present technique of shaping by means of a diamond hole cutter. Figure 2-1 shows, on the left, an InSb wafer that has been shaped and final-polished on the B-face, ready for CCIRID processing; and on the right, a completely processed wafer. Approximately 50 8585 chips/wafer are obtained on the 3.2-cm diameter slices.

A summary of the InSb material specifications is given in Table 2-1.

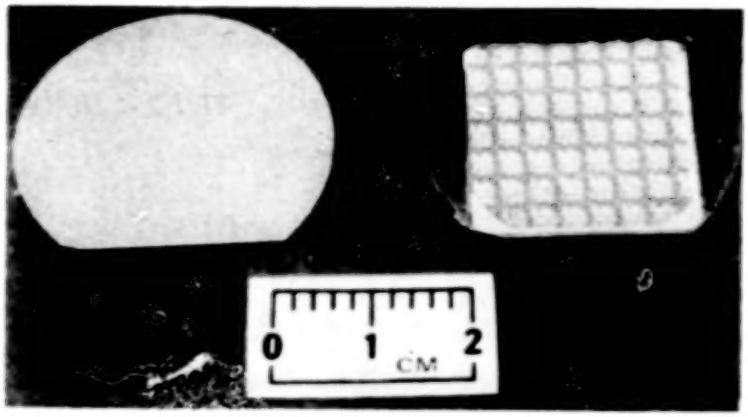

Figure 2-1. - InSb CCIRID Wafers.

Table 2-1. InSb Wafer Specification Summary

TYPE	CZOCHRALSKI SINGLE CRYSTAL, n-TYPE
DOPANT	UNDOPED
DIAMETER	32 ± 0.25 mm
FLAT LENGTH	21.17 ± 0.25 mm
THICKNESS	635 ± 25 μm
PARALLELISM	FACES PARALLEL TO WITHIN 25 μm
FLATNESS	FLAT TO WITHIN 5 μm WITHIN 28 mm CENTRAL DIAMETER
LINE DISLOCATIONS	<6 mm IN LENGTH
ETCH PIT DENSITY	$\leq 100/cm^2$
ORIENTATION	WITHIN $1/2^0$ OF (111)
SURFACE POLISH	<0.1 μm FINISH, B FACE <5 μm FINISH, A FACE
EDGE CHIPS	≤2 PER WAFER FACE
CARRIER CONCENTRATION N_D (77 K)	5.0×10^{13} TO $2.0 \times 10^{14}/cm^3$
ELECTRON MOBILITY μ_e (77 K)	≥525,000 cm^2/volt-sec

Interband Tunneling Considerations

Several factors influence the choice of N_D. The most important is tunnel current which motivates use of low carrier concentration material. It is generally realized that, for materials with bandgap below about 0.2 eV, interband tunneling presents a potentially important factor in device design and performance. InSb with its 0.228 eV energy gap represents a borderline case where tunneling is usually considered to be unimportant in, for example, InSb PV detectors where the impurity concentration of the substrate is sufficiently low to prevent tunnel diode characteristics and where the detector is operated with zero applied bias. However, the relatively high fields resulting at the surface when deep depletion conditions are established in an InSb CCD or CID can produce significant tunnel currents, particularly when the impurity concentration is high. For a given surface potential, the maximum surface electric field increases as $\sqrt{N_D}$ and, since the tunnel current density varies exponential with this electric field, a strong dependence of tunnel current on N_D results.

This tunneling current has been considered in detail by Anderson[3]. Referring to Figure 2-2, which shows an MOS structure with n-type substrate biased into a deep depletion condition, tunneling from the valence to the conduction band is possible for electrons with energy between E_{vo} and E_{cw}. After introduction of several approximations which, however, do not introduce errors of more than a few percent for tunnel current densities ≤ 0.1 amp/cm^2, the tunnel current may be written in the form

$$\frac{J_T}{q} \cong \frac{\left(q\psi_s - \frac{E_g}{2}\right) qF_{sc}}{\pi^3\sqrt{2}\,\hbar^2}\left(\frac{m^*_y m^*_z}{E_g^2}\right)^{\frac{1}{2}}\left(\frac{E_g}{m^*_x}\right)^{\frac{1}{2}} \times \frac{\left(\frac{b}{a}\right)^{\frac{1}{2}} \exp\left(-\frac{\sqrt{a/b}\,\pi}{2\sqrt{2}qF_{sc}\hbar}\sqrt{\frac{m^*_x}{E_g}}\,E_g^2\right)}{\left\{4 + \frac{\sqrt{a/b}\,\pi}{2\sqrt{2}qF_{sc}\hbar}\cdot\sqrt{\frac{m^*_x}{E_g}}\,E_g^2\right\}} \tag{2-1}$$

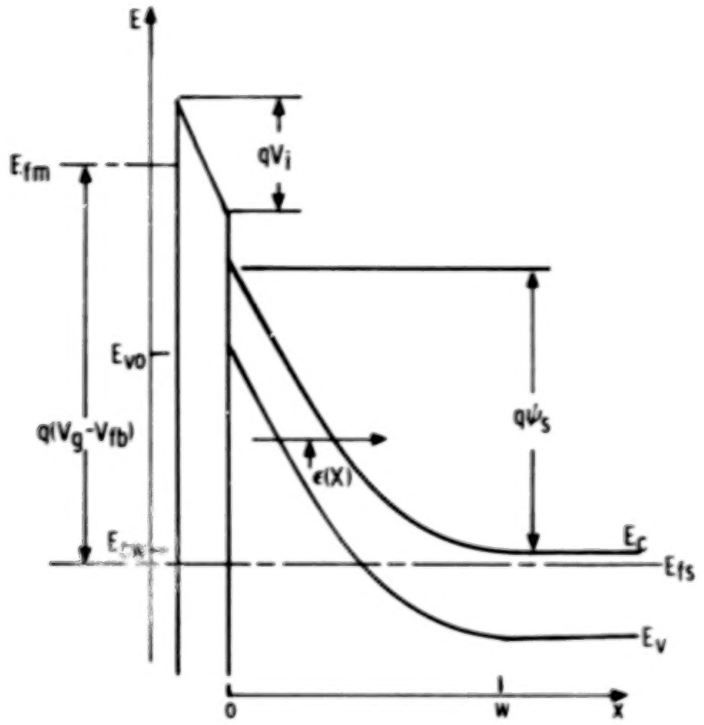

Figure 2-2. - Interband Tunneling in MOS Structure.

where

$$\frac{a}{b} \equiv \frac{q\psi_s}{q\psi_s - E_g/2} \,. \tag{2-2}$$

E_g is the bandgap, F_{sc} is the electric field and $\hbar$ the reduced Planck's Constant. The effective mass is isotropic in InSb with

$$\sqrt{\frac{m^*_i}{E_g}} = \frac{\sqrt{3}\,\hbar}{2P} \tag{2-3}$$

where i = x, y, z and P is an interband matrix element which, for InSb, is equal to

$$P = 1.440 \times 10^{-28} \text{ joule-meter.} \tag{2-4}$$

Evaluating the constant terms in equation (2-1):

$$C_1 \equiv \frac{q}{\pi^3\sqrt{2}\,\hbar^2}\left(\frac{m^*_y m^*_z}{E_g^2}\right)^{\frac{1}{2}}\left(\frac{E_g}{m^*_x}\right)^{\frac{1}{2}} \tag{2-5}$$

$$= \frac{q}{\pi^3\sqrt{2}\,\hbar^2}\;\frac{\sqrt{3}\,\hbar}{2P}$$

$$= 2.084 \times 10^{41}\ \text{coul/joule}^2\text{-sec-m}$$

and

$$C_2 \equiv \frac{\pi}{2\sqrt{2}\,q\,\hbar}\sqrt{\frac{m^*_x}{E_g}}\cdot E_g^2 \tag{2-6}$$

$$= 5.563 \times 10^7\ \text{volts/meter}$$

for $E_g = 0.228\ \text{eV} = 3.6526 \times 10^{-20}$ joule, allows rewriting (2-1) as

$$\frac{J_T}{q} \cong C_1\left(q\psi_s - \frac{E_g}{2}\right)F_{sc}\cdot\frac{\left(\frac{b}{a}\right)^{\frac{1}{2}}\exp\left(-C_2\sqrt{a/b}/F_{sc}\right)}{\left\{4 + \left(C_2\sqrt{a/b}/F_{sc}\right)\right\}} \tag{2-7}$$

To express J_T with ψ_s as the independent variable, use is made of the relation:

$$F_{sc} = C_3\left(q\psi_s\right)^{\frac{1}{2}} \tag{2-8}$$

where

$$C_3 \equiv \left(2N_D/\epsilon_s\right)^{\frac{1}{2}}. \tag{2-9}$$

Substituting (2-2) and (2-8) into equation (2-7) leads to the final result:

$$\frac{J_T(\psi_s)}{q} \cong \frac{C_1C_3\left(q\psi_s - \frac{E_g}{2}\right)^{3/2}}{\left\{4 + \frac{C_2}{C_3}\left(q\psi_s - \frac{E_g}{2}\right)^{-\frac{1}{2}}\right\}}\exp\left\{-\frac{C_2}{C_3}\left(q\psi_s - \frac{E_g}{2}\right)^{-\frac{1}{2}}\right\} \tag{2-10}$$

InSb tunnel current density versus surface potential for four values of impurity concentration N_D, calculated using equation (2-10), is plotted in Figure 2-3. The tunnel current is expressed as a carrier flux density (log scale) on the left-hand ordinate, and a current density on the right-hand ordinate. The extreme variation with N_D is apparent. At $|\phi_s| = 2$ volts, for example, the tunnel current varies 21 orders of magnitude between 2×10^{14} and $2.5 \times 10^{15}/cm^3$ carrier concentrations. For the latter value of N_D, J_T increases rapidly as ϕ_s only slightly exceeds the bandgap E_g. This is analogous to the rapid increase in reverse current of a backward diode. For $N_D = 2 \times 10^{14}/cm^3$, however, surface potentials of several volts are possible before appreciable tunneling occurs.

It is now necessary to relate the results of Figure 2-3 to limits on CCD operation. Although several relationships between dark current, clock frequency, and CCD performance can be developed, the most straightforward approach is to compare the tunnel current, J_T, with the thermally-generated current J_g in the device. The particular criterion applied is to determine the surface potential at which $J_T = J_g$.

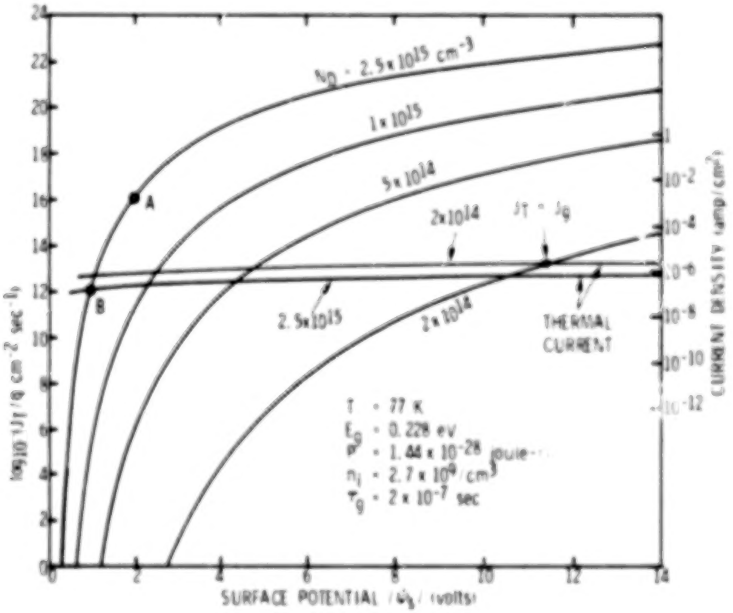

Figure 2-3. - Interband Tunnel Current versus Surface Potential for InSb.

With appropriate processing to minimize surface generation, it has been shown[1] that thermal generation in InSb MOS devices at 77 K is determined by bulk current sources and, in particular, by generation within the volume of the depletion region. This current is given by

$$\frac{J_g}{q} = \frac{n_i W}{\tau_g} = \frac{n_i}{\tau_g}\left(\frac{2\epsilon_s |\psi_s|}{qN_D}\right)^{\frac{1}{2}} \qquad (2\text{-}11)$$

where τ_g is the generation lifetime in the depletion region. τ_g has been obtained from Zerbst-plot analysis of InSb MOS capacitance-time plots, and is typically 0.2 μsec. Using this value in equation (2-11), the thermal generation currents have been plotted in Figure 2-3 for the two extreme values of N_D considered. Since $J_g \propto \sqrt{\psi_s}$, the thermal currents are nearly horizontal lines on the log plot of Figure 2-3.

The surface potentials at which $J_T = J_g$ are: $|\psi_s| = 1$ volt for $N_D = 2.5 \times 10^{15}/cm^3$; $|\psi_s| = 11.4$ volts for $N_D = 2 \times 10^{14}/cm^3$; and intermediate values for N_D between these two cases. These potentials represent the upper limit to surface potential in a CCD fabricated on InSb of that impurity concentration. Consider, for example, an InSb CCD fabricated on $N_D = 2.5 \times 10^{15}/cm^3$ material. Assume that a clock voltage is applied to a CCD gate with a magnitude so as to instantaneously establish an empty-well surface potential exceeding the potential at which $J_T = J_g$. For example, take $|\psi_s| = 2$ volts, point A in Figure 2-3. At this potential, tunnel current exceeds the thermal generation rate by four orders of magnitude, and the minority carriers generated will rapidly accumulate at the interface until the surface potential is reduced to 1 volt (point B), at which point the normal thermal process is resumed. Therefore, for this particular impurity concentration, attempts to clock the CCD so as to produce $|\psi_s| > 1$ volt under any gate will produce large tunnel currents which will quickly return the potential to 1 volt. For the low concentration $N_D = 2 \times 10^{14}/cm^3$, a wide range in CCD surface potentials (about 11 volts) is possible before the tunneling process begins.

Since charge storage capacity is directly related to maximum surface potential, as N_D is increased progressively smaller charge capacity results until charge transfer ceases completely (the specific limiting impurity concentration depending on whether the CCD is 2¢ or 4¢). Based on these calculations, which have been verified by experimental determination of the onset of tunneling in InSb MOS capacitors, material with N_D no higher than $2 \times 10^{14}/cm^3$ was used for device fabrication. Resulting CCD charge capacities are in excess of 10^6 holes. Since tunneling is a basic quantum mechanical limitation, it is not unique to InSb, and comparable tunnel currents occur in other direct gap materials having the same bandgap.

8585 CHIP DESIGN AND DESCRIPTION

In earlier work[1,2] shift registers were fabricated in InSb to demonstrate the feasibility of CCDs in this material. These made use of the then-available processing technology, one based on gold metallizations and SiO dielectric layers. Due to the relative difficulty in etch delineation of these materials, device dimensions were limited. CCDs with 50-μm and 25-μm gate lengths were fabricated for which CTEs of 0.9 and 0.975 per transfer, respectively, were measured. A further limitation was encountered with the on-chip p-n junctions, which were formed by a mesa technique; the non-planarity of the diodes prevented their reduction to the required size and reduced yields in the dielectric deposition steps.

In this program, a new InSb CCIRID chip was successfully fabricated based on an improved process which eliminates the limitations inherent with the earlier techniques. This process includes planar junction formation and an aluminum and SiO_2 material system which is amenable to state-of-the-art delineation techniques.

The monolithic InSb chip is designated the SBRC 8585; a photomicrograph of a die from a completed wafer is shown in Figure 2-4. The principal device on the chip is a 20-element CCIRID (center). Smaller complementary

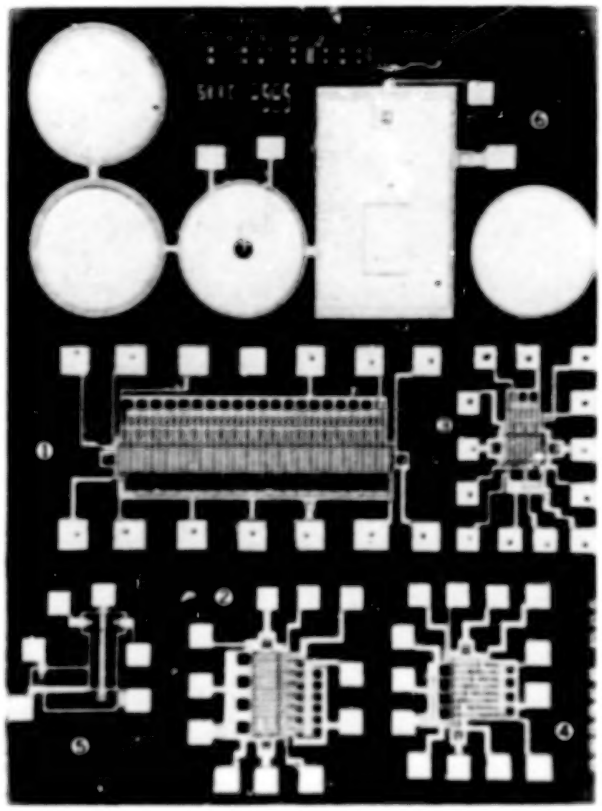

Figure 2-4. - Monolithic InSb CCIRID Chip (SBRC 8585).

devices are two- and four-element CCIRIDs, which differ in design details, and a four-element TDI array with tapered register. The balance of the chip contains MOS capacitors and gate-controlled diodes for process diagnostics. The various devices are numbered in Figure 2-4 as follows:

1. 20-element linear imager
2. 4-element linear imager
3. 2-element linear imager
4. 4-element TDI array
5. Monolithic Gated Charge Integrator (GCI)
6. Test devices

Device numbers 1, 3, and 4 are all 4¢ devices, with 12.5-μm (0.5-mil) gate lengths in the cases of 1 and 4; device 3 has 10.0-μm (0.4 mil) gate lengths. Device number 2 is a 2¢ structure with 12.5-μm gate lengths. The test

devices consist of three capacitors with different gate metal - either channel stop, buried, or surface metal. There are, in addition, two gated diodes to aid in evaluating process parameters. The 8585 chip dimensions are 2388 μm (94 mils) by 2896 μm (114 mils). The design rules for the 8585 chip are shown in Table 2-2.

Table 2-2. - 8585 Chip Design Rules.

DIMENSION	MINIMUM DIMENSION ON SBRC 8585 (mils)
CHANNEL STOP WIDTH	0.20
ALUMINUM LINE WIDTH (ANY LEVEL)	0.20
AL-TO-AL GAP (ANY LEVEL)	0.20
SM-TO-BM OVERLAP	0.125
GATE LENGTH	0.40
CONTACT WINDOWS	0.3 X 0.8
SOURCE-DRAIN IMPLANT WIDTH FOR ARRAY DIODES	2.0

A schematic cross section perpendicular to the channel for the CCIRIDs on the 8585 chip is shown in Figure 2-5. The design/dimensions of the 20-element CCIRID are specified here, but the design of all the devices on the 8585 is similar. The 20-element CCIRID incorporates an array of 20 MOS detectors. The accumulated detector charges are transferred laterally into an opaque InSb shift register by means of a surface metal transfer gate (ϕ_T). A separate detector array rather than detection in the CCD channel provides greater flexibility since detector integration times may be varied independently of CCD clock frequency. The MOS photogates are 35 by 32.5 μm on 50-μm centers and are biased via a common bus bar (ϕ_p). 75Å of evaporated titanium was used as the semitransparent photogate material. The IR transmittance of the thin Ti gate structure was measured to be 38% including

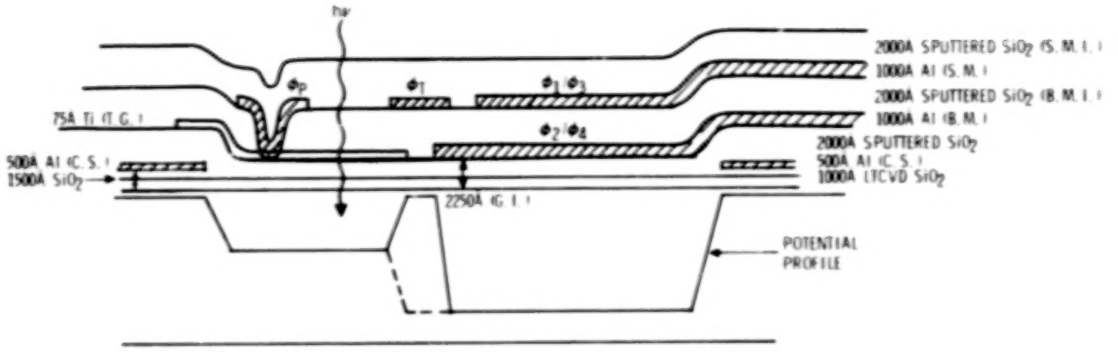

Figure 2-5. - Cross Section Perpendicular to Channel for CCIRIDs on SBRC 8585 Chip.

reflection losses associated with the oxide layers above and below it. Ti was used for convenience and an improved transparent gate structure having lower loss is being developed.

The 20-bit shift register is a 4¢, surface channel, overlapping gate CCD. The gate oxide of the CCD is 1000Å of SiO_2 grown on the InSb wafers by low-temperature chemical vapor deposition (LTCVD) using silane and oxygen at ~ 200°C. An additional 500Å thick layer of SiO_2 is sputter deposited over the LTCVD SiO_2 layer, which passivates the gate oxide and serves as a transition layer between the LTCVD oxide and the other oxide and aluminum layers in the CCD structure, which are all sputtered. Aluminum gates and oxide contact cuts are delineated by chemical and plasma etching, respectively. The gate length on the 20-element device is 12.5 μm.

The 8585 chip incorporates planar p^+-n junctions formed by ion implantation of beryllium for FZ input and charge output. The availability of a compatible junction technology may enable additional features to be incorporated in future chip designs such as overload protection or ac-coupled detector inputs. The implanted InSb junctions have sufficiently high breakdown voltage and low leakage for use in infrared CCD devices. Their breakdown voltage increases as N_D^{-1} and is greater than 5 volts for the impurity concentrations considered. Figure 2-6 shows a 77 K I-V characteristic for a Be-implanted diode on InSb with $N_D = 4.5 \times 10^{14}/cm^3$, with breakdown

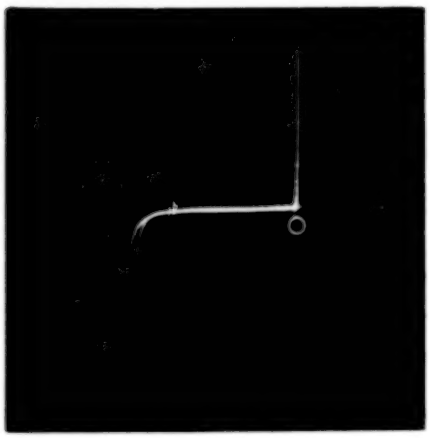

Figure 2-6. - I-V Characteristic of Implanted Planar InSb p-n Junction (T = 77 K, N_D = 4.5 × 10^{14}/cm^3; 2 volts/div; 10 μa/div).

voltage of 8 volts. The forward and reverse currents of the implanted InSb junctions have been analyzed and found to follow the usual theory for abrupt junctions, with recombination-generation current dominating at 77 K. At 1-volt reverse bias, the 77 K reverse current density is 5 × 10^{-7} amp/cm^2. This low leakage permits use of the Be-implanted junctions as the output diode in a floating diffusion output circuit.

PROCESS DESCRIPTION

A total of fourteen mask levels is used to fabricate the 8585 CCIRID devices. The block diagram of Figure 2-7 illustrates the processing steps for the 8585 InSb CCIRID chip. The processes designated in Figure 2-7 are explained according to process step, layer designation, process description, and the process control methods used in Table 2-3.

As can be seen in Table 2-3, processing of the CCIRID devices requires the use of five different metal depositions: sputter deposition of aluminum for the channel stop, buried, surface and pad metal layers; and the use of thermally-deposited titanium for the semitransparent gates. The insulating layers in the CCIRID structure require five different oxide depositions.

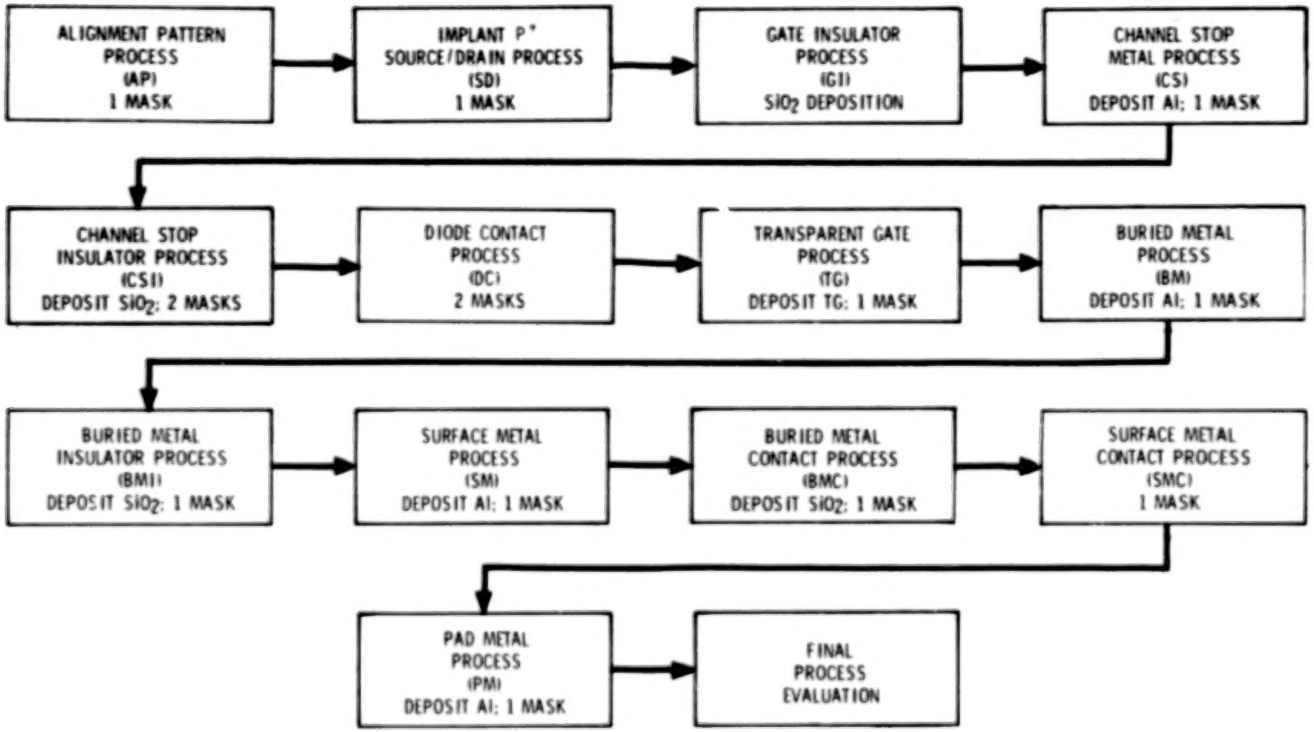
ALIGNMENT PATTERN PROCESS (AP) 1 MASK
IMPLANT P+ SOURCE/DRAIN PROCESS (SD) 1 MASK
GATE INSULATOR PROCESS (GI) SiO2 DEPOSITION
CHANNEL STOP METAL PROCESS (CS) DEPOSIT Al; 1 MASK
CHANNEL STOP INSULATOR PROCESS (CSI) DEPOSIT SiO2; 2 MASKS
DIODE CONTACT PROCESS (DC) 2 MASKS
TRANSPARENT GATE PROCESS (TG) DEPOSIT TG; 1 MASK
BURIED METAL PROCESS (BM) DEPOSIT Al; 1 MASK
BURIED METAL INSULATOR PROCESS (BMI) DEPOSIT SiO2; 1 MASK
SURFACE METAL PROCESS (SM) DEPOSIT Al; 1 MASK
BURIED METAL CONTACT PROCESS (BMC) DEPOSIT SiO2; 1 MASK
SURFACE METAL CONTACT PROCESS (SMC) 1 MASK
PAD METAL PROCESS (PM) DEPOSIT Al; 1 MASK
FINAL PROCESS EVALUATION

Figure 2-7. Process Flow Chart for 8585 InSb CCIRID.

Table 2-3. 8585 CCIRID Fabrication Steps

PROCESS STEP	STEP DESIGNATION	PROCESS DESCRIPTION	PROCESS CONTROL METHODS
A: ALIGNMENT PATTERN	AP	ETCH BASIC ALIGNMENT MARKS INTO SUBSTRATE	MICROSCOPIC INSPECTION FOR SIZE AND EDGE DEFINITION.
SOURCE/DRAIN p^+ IMPLANT	SD	ION IMPLANT p^+ BERYLLIUM THROUGH PHOTORESIST PATTERN	MICROSCOPIC INSPECTION OF STAINED WITNESS SAMPLES.
B: GATE INSULATOR	GI	DEPOSIT SILICON DIOXIDE GATE INSULATOR	CAPACITANCE VERSUS VOLTAGE TO CHARACTERIZE ELECTRICAL PROPERTIES OF SILICON DIOXIDE - INDIUM ANTIMONIDE INTERFACE, INCLUDING SURFACE STATE DENSITY, STORAGE TIME, FLAT BAND SHIFT, HYSTERESIS AND CAPACITANCE.
C: CHANNEL STOP METAL	CS	SPUTTER DEPOSIT ALUMINUM METALLIZATION AND ETCH	SURFACE PROFILOMETER MEASUREMENT OF THICKNESS. MICROSCOPIC INSPECTION OF GEOMETRY AFTER ETCHING.
CHANNEL STOP INSULATOR OR FIELD OXIDE	CSI OR FO	SPUTTER DEPOSIT SILICON DIOXIDE INSULATOR AND ETCH	GEOMETRY AFTER ETCHING; THICKNESS MEASUREMENTS.
DIODE CONTACT	DC	ETCH INSULATORS TO IMPLANTED InSb SURFACE AND FORM DIODE CONTACT	GEOMETRY AFTER ETCHING; ELECTRICAL SHORT PROBE TESTS; 77°K DIODE PROBE TESTS.
TRANSPARENT GATE	TG	THERMALLY DEPOSIT TITANIUM THROUGH PHOTORESIST MASK	GEOMETRY; TRANSMISSION, ABSORPTION AND REFLECTIVITY OF WITNESS SAMPLES.
BURIED METAL	BM	SPUTTER DEPOSIT FIRST ALUMINUM CCD GATE METALLIZATION AND ETCH	GEOMETRY AFTER ETCHING; THICKNESS MEASUREMENTS.
BURIED METAL INSULATOR	BMI	SPUTTER DEPOSIT BURIED, AND SURFACE GATE INSULATOR AND ETCH CONTACT WINDOWS	GEOMETRY AFTER ETCHING; THICKNESS MEASUREMENTS.
SURFACE METAL	SM	SPUTTER DEPOSIT SECOND ALUMINUM CCD GATE METALLIZATION AND ETCH	GEOMETRY AFTER ETCHING; THICKNESS MEASUREMENTS.
SURFACE METAL INSULATOR AND BURIED CONTACTS	BMC	SPUTTER DEPOSIT SURFACE METAL SILICON DIOXIDE INSULATOR AND ETCH BURIED METAL GATE CONTACTS	GEOMETRY AFTER ETCHING; THICKNESS MEASUREMENTS OF INSULATOR.
SURFACE METAL CONTACTS	SMC	ETCH SURFACE METAL GATE CONTACTS	GEOMETRY AFTER ETCHING.
PAD METAL	PM	SPUTTER DEPOSIT ALUMINUM AND ETCH BOND PADS	GEOMETRY AFTER ETCHING; THICKNESS MEASUREMENTS.
D: FINAL PROCESS EVALUATION		MECHANICAL AND ELECTRICAL INTEGRITY DETERMINED BY MICROSCOPIC INSPECTION, ELECTRICAL PROBE TESTS, SURFACE C-V TESTS, AND DIODE C-V TESTS. SCANNING ELECTRON MICROSCOPE FOR HIGH-MAGNIFICATION INSPECTION OF MULTILAYER STRUCTURE, VOLTAGE CONTRAST EVALUATION, AND VOLTAGE BREAKDOWN STUDIES	

These include the deposition of LTCVD SiO_2 for the gate insulator to obtain the required low surface state density. The LTCVD SiO_2 layer is sealed with an overcoating of sputtered SiO_2. Sputtered SiO_2 is also used for the channel stop, buried metal and surface metal insulating layers.

The process utilizes positive photoresist (Shipley AZ1300 series) and 2:1 reduction project on mask aligning to delineate the CCD devices. Etching of the aluminum gate patterns is done chemically while contact cuts through the oxide layers are etched with a plasma etcher/asher.

MASK AND PROCESS MODIFICATIONS

The original 8585 mask design had some features which were found to be incompatible with the actual processing sequence for fabricating the CCIRIDs as it developed during the program. These design changes led to new photomasks being fabricated for the channel stop insulator, surface metal insulator, and diode contact levels.

The first mask change required was to separate the channel stop metal contact window cuts from the channel stop insulator etch process (CSI). In the CSI etch step, the total thickness of the oxide is reduced in the CCD channel region. In this operation only a fraction of the oxide is removed and no absolute stop point (i.e., an underlying metal layer) is reached. The CSI step is intended to reduce the oxide thickness in the channel so as to decrease the clock voltage magnitudes required to operate the CCD. A result of the CSI etch is that some oxide remains in the channel stop metal contact window. By adding a new mask designated CSC, these contacts are now separately etched through to the metal stop to assure continuity.

The second mask change required separation of the BMC and SMC contact window cuts in place of the original SMI etch mask. This change was found to be necessary because of the different oxide thicknesses involved. The oxide overlying the surface metal is 0.2 μm thick while the oxide over the buried metal is 0.4 μm thick. When both sets of contact cuts were etched

simultaneously with the original mask, the surface metal contact cuts were severely overetched while clearing the buried metal contact cuts.

CCIRID wafers which were processed early in the contract were found to have a high number of "open" p-n junctions (input and output diodes) which were due to various degrees of contact degradation. This degradation varied from oxide lifting around the contact windows, to windows which appeared visually acceptable but were electrically open. Junctions tested for contact continuity at room temperature showed contact resistances which ranged from > 1000 MΩ (opens) to ~ 40Ω. When cooled to 77 K, all were found to either open or show very poor forward characteristics.

The scanning electron microscope (SEM) was used to determine why the diode contacts were opening. The SEM photograph shown in Figure 2-8 illustrates the origin of the contact failures. The photograph clearly shows that while the overlying aluminum conductor is continuous over the upper oxide

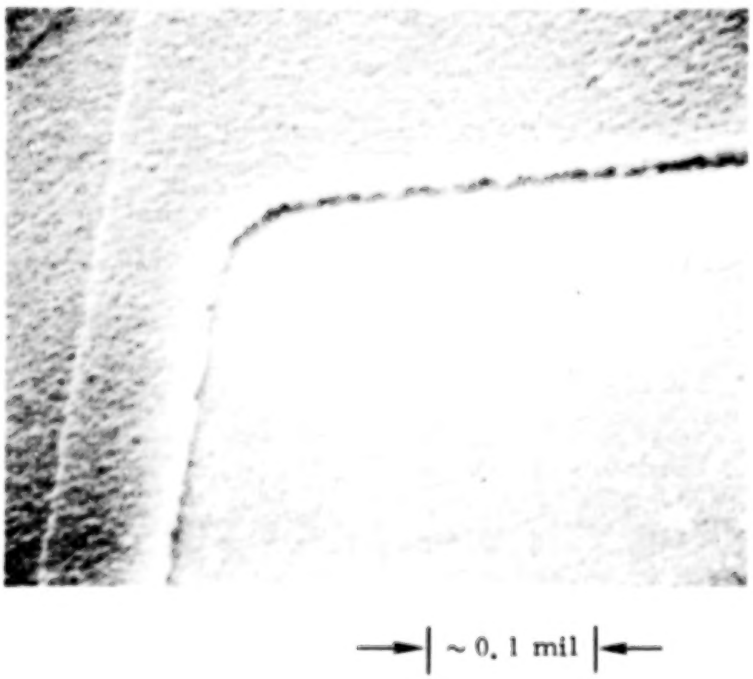

Figure 2-8. - SEM Photograph of Etched Diode Contact Window Showing Undercutting of Gate Oxide Layer.

edge, it is discontinuous at the bottom edge indicating that the oxide layer is undercut at the InSb/SiO_2 interface. This was found to result from differential etch rates of the LTCVD SiO_2 gate insulator and the overlying sputtered SiO_2 field oxide. For the early wafer lots the diode contact windows were formed by etching through both oxide layers to the p-n junction surface in a single etching operation. The reason for this etch variation is that the LTCVD SiO_2 etches faster than the overlying sputtered SiO_2 (approximately 250Å/min versus 90Å/min, respectively. This variation in etch rate allows the gate oxide to etch faster laterally than the field oxide layer, thus creating an undercut profile at the lower oxide edge. This edge profile is shown schematically in Figure 2-9(A).

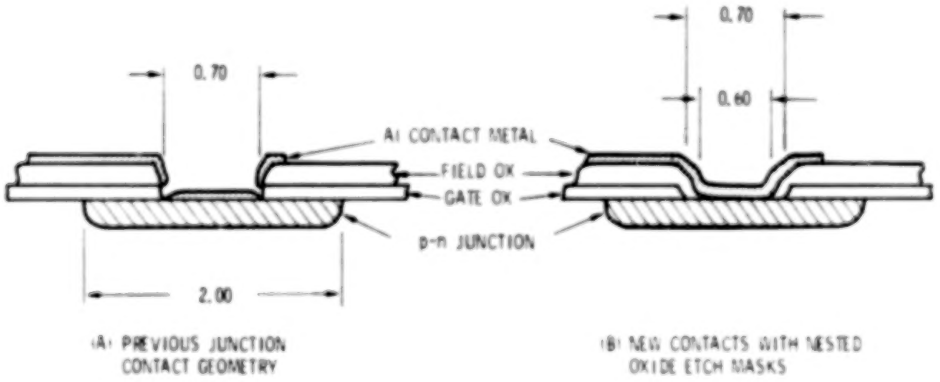

Figure 2-9.- p-n Junction Contacts on 8585 Chip (Dimensions for 20-Element Imager, in mils).

The solution to the diode contact problem required fabricating a new photomask which is identical to the original diode contact window mask except that the window dimensions are smaller by 0.10 mil per side, as shown in Figure 2-9(B). The process was changed so that following the channel stop metal delineation process, the original mask is used to etch contact windows through the gate oxide. Then the field oxide is deposited and the new smaller contact windows are etched. The "nested" etch masks result in a window geometry illustrated schematically in Figure 2-9(B). Since each oxide layer is etched separately, the lateral undercutting which occurs does not effect the

overall contact window. A SEM photograph of a typical contact processed with the nested oxide etch mask procedure is shown in Figure 2-10, showing continuous Al metal coverage of the window edges. Since implementation of the nested contact process, the yield of good diode contacts has exceeded 90%.

With these mask and process changes having been made, testable InSb CCIRIDs were produced beginning with 8585 Lot 4. The following sections describe the test results.

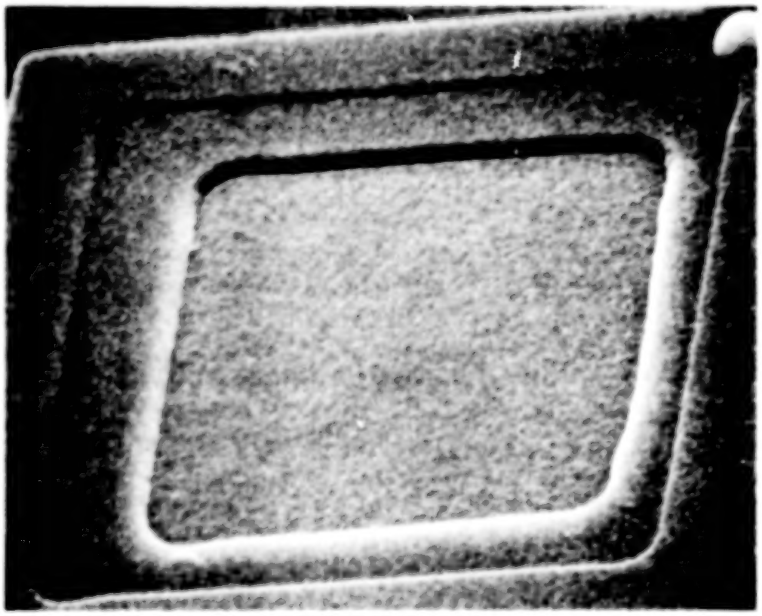

Figure 2-10.- SEM Photograph of Diode Contact Using Nested Oxide Etch Masks (2-Element CCIRID No. 498-20-B5, Lot 8B, 40°, 3500X).

Section 3

TWO-ELEMENT InSb CCIRID

DEVICE DESCRIPTION

The first device on the 8585 chip successfully processed and tested was the two-element, 4¢ InSb CCIRID. This CCD is at the center right in Figure 2-4. It is a smaller version of the 20-element CCIRID and is basically similar to it in design. The two-element device was included on the chip to take advantage of its higher yield due to its smaller device area, optimizing the possibility of obtaining CCD data from the 8585 chip as early as possible.

A photomicrograph of the two-element CCIRID is shown in Figure 3-1. The CCD register is at the center of the photograph and the two dark square regions to the right of the CCD channel are the MOS detectors (photogates). The input and output p-n junctions are at the top and bottom of the photograph, respectively.

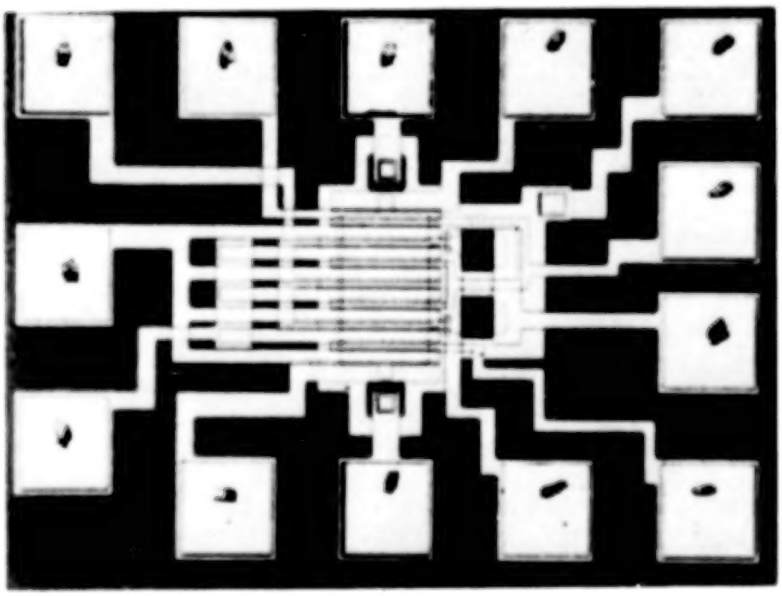

Figure 3-1. - Two-Element, 4¢ InSb CCIRID on 8585 Chip.

The schematic diagram for the two-element CCIRID is shown in Figure 3-2. The schematics for the two-element and 20-element CCIRIDS are identical and this figure will be referenced again in Section 4. The shift register in the two-element array is an overlapping-gate, 4ϕ device with 14 clocked gates (3-1/2 bits, 4 gates/bit). The first clocked gate is ϕ_2 and the last clocked gate is ϕ_3. The fat zero input (which can be also used to electrically input signal charge into the register) consists of a diode (V_{ID}), an input buried gate (V_{IB}), and an input surface gate (V_{SC}). The output elements consist of a diode, a buried metal output gate (V_{OG}), and a floating gate (ϕ_F) which may be optionally used.

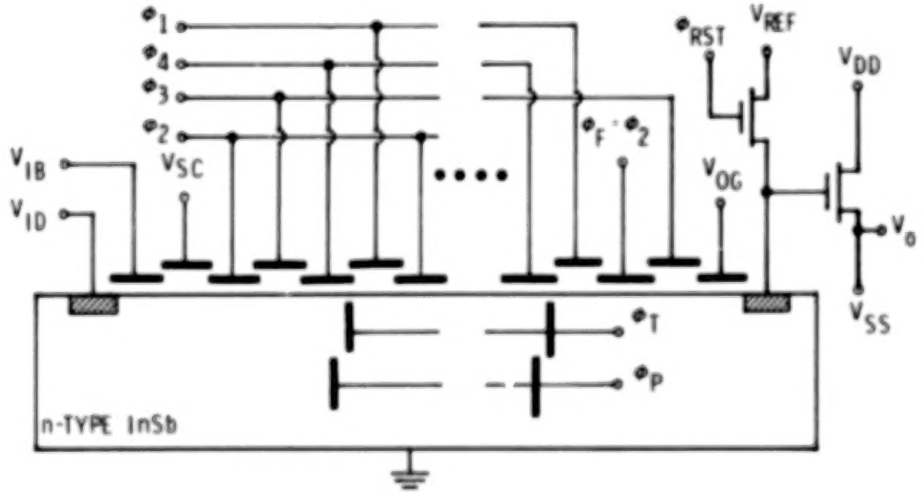

Figure 3-2. - Schematic Diagram of Two-Element and 20-Element InSb CCIRIDs.

Either the output p-n junction or the floating gate can be used for charge detection; in testing to date, the former approach has been taken, using the output junction in a floating diffusion output circuit. The circuit utilizes two 3N163 p-channel enhancement-type silicon MOSFETS, mounted in the flatpack adjacent to the InSb chip, for the source follower and switch transistors shown in Figure 3-2. An identical arrangement was used for the 20-element evaluation described in Section 4. All CCDs on the 8585 chip,

including the two-element device, also have a floating clock output option. Operating with the floating diffusion output, the isolated gate ϕ_F, which lies between a ϕ_1 and ϕ_3 gate, was tied to its appropriate phase (ϕ_2) and clocked normally.

The device has two photogate detectors biased through a common bus (ϕ_P) and a surface metal transfer gate (ϕ_T). The photocharge from the detectors enters the register through two ports in the channel stop metal beneath ϕ_4 gates. The ports are one and three bits away from the output; i. e., there is an empty (isolation) bit between detector inputs. This differs from the 20-element CCIRID which has one CCD bit/detector. The CCD gate length in the two-element device is 10 μm, slightly smaller than that in the 20-element device (12.5 μm). With these exceptions the device layouts are identical.

GATE OXIDE WITNESS EVALUATION

Several two-element CCIRIDs were tested from wafer number* 442-14, 8585 Lot 4. Each wafer lot includes a witness wafer for evaluating the gate oxide characteristics after deposition but prior to subsequent CCD processing, and p-n junction characteristics. The gate oxide witness for 8585 Lot 4 was sample number 486A-10A. The witness is processed simultaneously with the CCIRID wafers up through sputtering of the 500Å SiO_2 overlayer. In the deposition of the first device metal layer (the channel stop metal layer) the CCIRID wafers are removed from the system after 500Å of Al is deposited. The witness wafer remains to receive a total of 2000Å for ease of wirebonding to the test capacitors. In this manner the witness undergoes identical process conditions through the first gate level. The witness wafers are drawn from the inventory of wafers not suitable for CCIRID processing (e. g., those with

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*The device identification system used throughout this report is as follows: Each CCD chip is identified by a seven-digit number as: XXX-XX-XX. The first three numbers represent the InSb ingot number; the second two the wafer number; and the last pair (alphanumeric) identifies the particular chip or die.

scratches or too high an impurity concentration). The 2000Å of aluminum on the witness wafer is photoetched into a pattern of 20-mil diameter dots. After dicing into groups of nine dots, chips are mounted in TO-5 packages which adapt to specially-designed MOS capacitor evaluation dewars.

The witness capcitors are evaluated for flatband voltage, surface state density, and other parameters pertinent to the CCIRIDs. To allow rapid accumulation of the necessary C-V and other MOS diagnostic data, a computer-aided surface analysis system has been used in this program. A survey to determine the optimum N_{ss} measurement technique for InSb and other infrared semiconductors, resulting in selection of the quasi-static technique, and design and setup of the automated C-V system, was accomplished on a related contract (F04701-76-C-0174). The system has been continually improved and its capabilities expanded under SBRC's Two-Dimensional Infrared Array IR&D Project. Its present configuration is shown in Figure 3-3. In addition to its principal output, N_{ss} versus surface potential, software for N_{ss} measurement by the conductance method, substrate impurity concentration calculation, and C-t data acquisition and analysis has been implemented. Not shown in Figure 3-3 are a PAR 135 Electrometer, an HP 3310A Function Generator, and a Tektronix 7403N Oscilloscope which are used in obtaining the quasi-static (low-frequency) capacitance characteristics and the pulsed capacitance (C-t) data.

Figure 3-4 shows the measured low-frequency and high-frequency C-V characteristics (dashed curves) for one (typical) capacitor from the Lot 4 witness sample. The solid curve is the ideal low-frequency C-V characteristic calculated by the computer for the particular impurity concentration and oxide capacitance of the witness sample. The oxide capacitance from the accumulation region of the curve is 43pf giving $C_{OXW} = 43pf/2.03 \times 10^{-3} cm^2 = 2.12 \times 10^{-8} f/cm^2$. The measured thickness of the LTCVD SiO_2 plus sputtered overlayer was 1650Å giving for the calculated dielectric constant of the witness gate oxide:

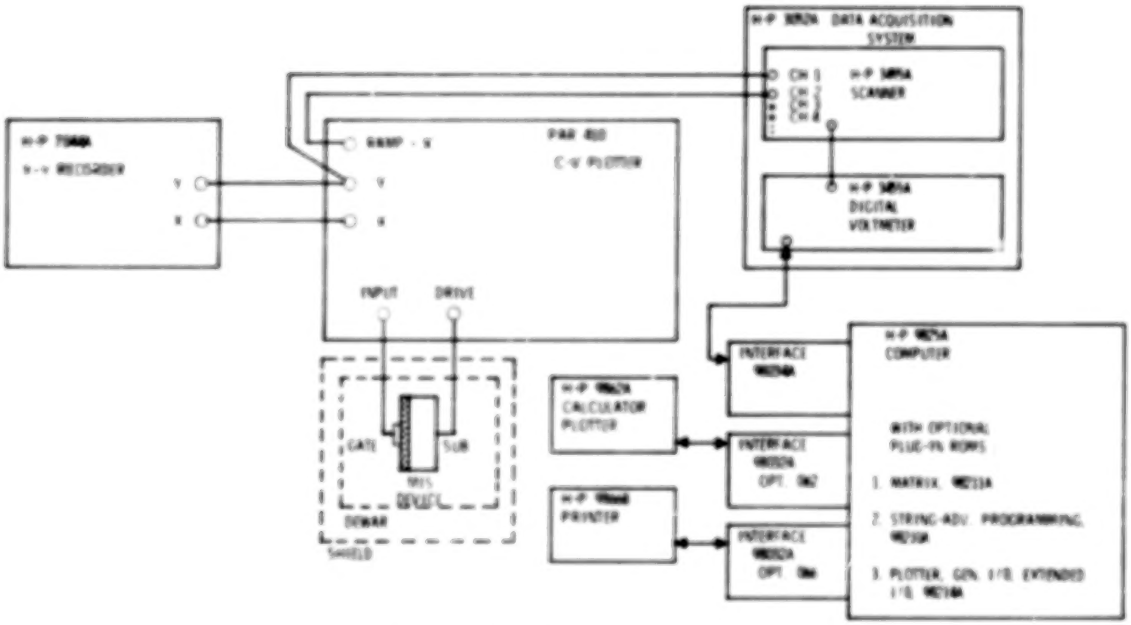

Figure 3-3. - SBRC Capacitance Measurement System.

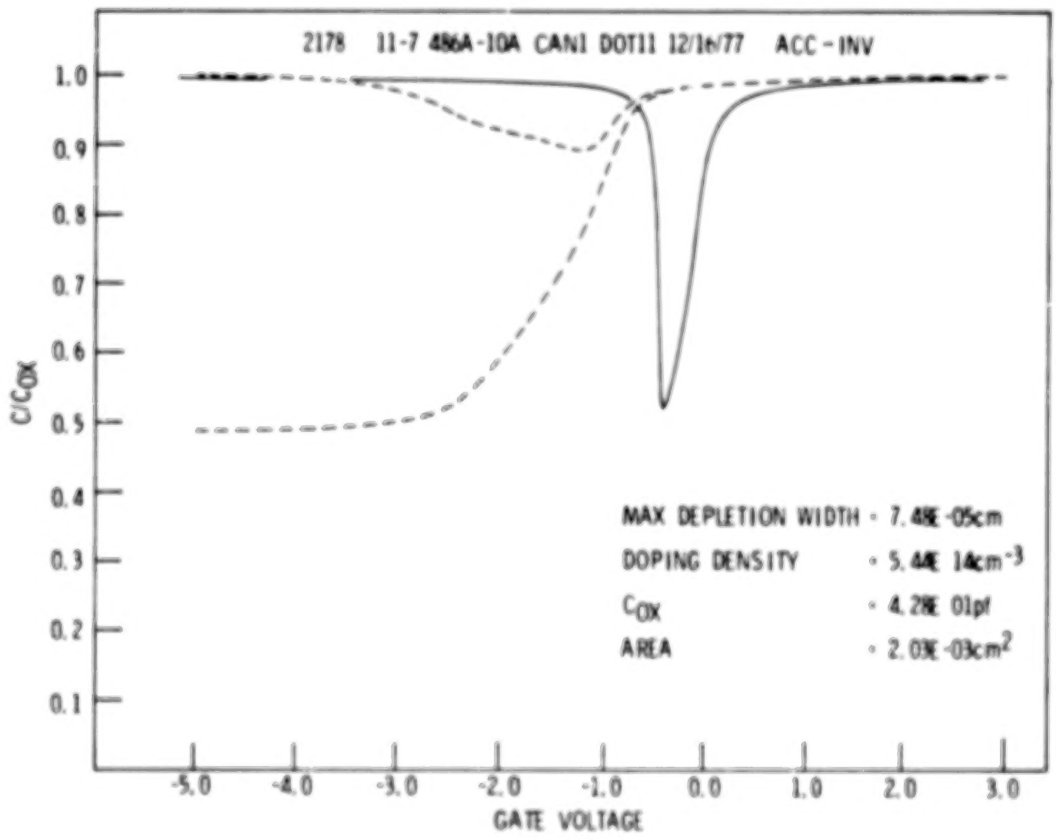

Figure 3-4. - Low-Frequency and High-Frequency C-V Curves for Gate Oxide Witness; 8585 Lot 4; Sample 486A-10A.

$$K_{OXW} = \frac{C_{OXW}\, t_{OXW}}{\epsilon_o} = 3.95 \qquad (3\text{-}1)$$

in excellent agreement with the expected dielectric constant of SiO_2.

The flatband capacitance can be obtained from the C-V computer program or the equation

$$\frac{C_{FB}}{C_{OX}} = \left[1 + C_{OX}\left(\frac{kT}{N_D \epsilon_s q^2}\right)^{\frac{1}{2}}\right]^{-1} \qquad (3\text{-}2)$$

which gives $C_{FB} = 0.87\, C_{OX}$ for the witness sample parameters. For the capacitor of Figure 3-4, the flatband voltage is -1.0 volt. Average V_{FB} of all samples was -1.15 volts. The net fixed charge density at the interface may be then calculated as

$$N_{fc} = Q_{fc}/q \cong C_{OXW}\,(-V_{FB})/q = +1.5 \times 10^{11} \text{ charges/cm}^2 \qquad (3\text{-}3)$$

This low fixed (positive) charge density is characteristic of the LTCVD SiO_2 - InSb interface, and leads to relatively low clock voltage requirements for the CCIRIDs. Note that the calculation (3-3) assumes zero metal-semiconductor work function difference (Φ_{MS}). Taking handbook photoelectric work functions for Al and InSb indicates that Φ_{MS} may be as large as -0.5 volt, but our data indicate that it is closer to zero (photoelectric work functions must be viewed as an estimate only of the actual work function difference in an MOS structure). The work function difference is expected to be negative, however, leading to an even lower N_{fc} than calculated in (3-3).

Referring again to Figure 3-4, the dispersion of the measured high-frequency capacitance curve relative to the ideal curve, and the small dip in the measured low-frequency curve, both indicate that N_{ss} is relatively high. Figure 3-5 shows the results of the quasi-static calculation of N_{ss}, showing a midband value of $10^{12}/\text{cm}^2\text{-eV}$. The LTCVD SiO_2 for 8585 Lot 4 was deposited in a vertical-flow configuration reactor, and this surface state density is to date typical of this particular reactor. CVD reactor comparisons

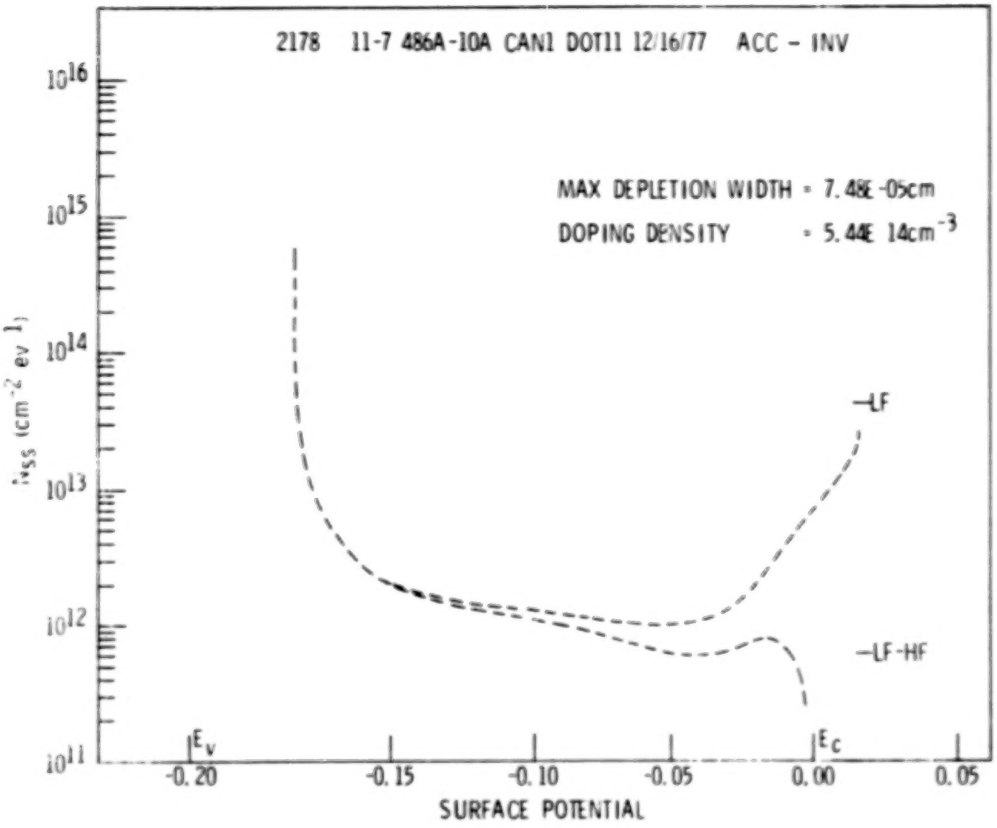

Figure 3-5.- Surface State Density of Gate Oxide Witness; 8585 Lot 4; Sample 486A-10A.

and a more detailed discussion of InSb gate oxide characteristics will be found in Section 5 and cited references.

Finally, although the witness sample dots were not stressed to destruction to determine ultimate breakdown strength, all dots withstood 20 volts bias, or 1.2×10^6 v/cm. Scaling this result to the nominal oxide thicknesses under the BM and SM of the CCD (2750Å and 4750Å respectively) these gate levels should withstand biases (with respect to substrate) of 33 and 57 volts respectively. This assumes no process-related degradation of oxide quality.

CCD GATE CAPACITANCE AND FLATBAND VOLTAGE

After completion of CCD processing, three MOS capacitors on each 8585 die are available for evaluation (see Figure 2-4). These capacitors are on the channel stop metal, buried metal, and surface metal levels so that the characteristics of each gate level may be determined. Flatband voltages of each gate level are measured to determine starting points for setting the clock voltages. The oxides beneath each of these three capacitors undergo the same processing conditions (e.g., etching) as their corresponding oxide levels in the CCD structures. Therefore, the capacitors provide an accurate measure of the CCD gate characteristics.

The oxide parameters for 8585 Lot 4, determined from the test capacitors, are tabulated in Table 3-1. Listed are the measured characteristics for the three gate levels along with the gate oxide witness sample. Row (a) in the table lists the nominal oxide thicknesses (total) under each gate level. The thicknesses for the various layers in the CCD are determined by Dektak stylus profilometer measurement of a step etched through the oxide layer. To provide a substrate which is inert to the oxide etch for accurate oxide thickness determination, single-crystal sapphire substrates are used for these witness parts. The density and thickness of the SiO_2 sputtered on the sapphire may differ slightly from that deposited on the InSb wafers; consequently, these thicknesses are "nominal" but close to the actual thicknesses on the InSb.

Row (b) in Table 3-1 gives the measured capacitance per unit area determined from the capacitor C-V curves and the known area of each dot. Using the dielectric constant (3.95) determined for the gate oxide witness sample and assuming* it is constant for each SiO_2 layer in the CCD, the oxide thicknesses may be calculated from the measured capacitances in row (b). The values so obtained should agree well with the nominal thick-

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*This is a valid assumption based on independent measurements of the dielectric constant of our sputtered SiO_2 films in MIM structures.

Table 3-1. Oxide Parameters, 8585 Lot 4.

	GATE OXIDE WITNESS	CHANNEL STOP METAL	BURIED METAL	SURFACE METAL
WAFER NO.	486A-10A	442-14	442-15	442-14
(a) NOMINAL OXIDE THICKNESS (Å)	1650	1650	2750	4750
(b) MEASURED C_{OX} (f/cm^2)	2.12×10^{-8}	2.13×10^{-8}	1.36×10^{-8}	7.79×10^{-9}
(c) DIELECTRIC CONSTANT	3.95	(3.95)	(3.95)	(3.95)
(d) CALCULATED OXIDE THICKNESS (Å)	--	1640	2580	4490
(e) ERROR (d) TO (a) (%)	--	-0.6	-6.2	-5.5
(f) FLATBAND CAPACITANCE (C_{FB}/C_{OX})	0.87	0.80	0.87	0.92
(g) MEASURED V_{FB} (volts)	-1.15	-0.8	-2.0	-4.0
(h) N_{fc} (charges/cm^2)	$+1.5 \times 10^{11}$	$+1.1 \times 10^{11}$	$+1.7 \times 10^{11}$	$+1.9 \times 10^{11}$

nesses in row (a). These are listed in row (d) and are seen to be quite close to the nominal values.

The flatband capacitances and measured flatband voltages for the CCD gate levels are listed in rows (f) and (g) of Table 3-1. Using equation 3-3, N_{fc} was calculated for each level [row (h)] and is seen to be in the 1 to 2 × $10^{11}/cm^2$ range consistent with the gate oxide witness sample. It should be noted that, for the LTCVD SiO_2-InSb interface, we have found[4] that the flatband voltage can be shifted either positive or negative by biasing the gate with respect to substrate prior to and during cooldown of the device to 77 K. These bias stress studies indicate the fixed charge results from injection from the semiconductor into the oxide. However, once cooled to 77 K, the

fixed charge remains constant under normal operating biases. The flatband voltages and corresponding fixed charge values given in Table 3-1 were measured with the gates floating during cooldown, rather than with any bias applied. In the InSb CCD testing throughout the program, the device terminals were also floated during cooldown so that the "intrinsic" fixed charge levels listed in Table 3-1 are the values that apply to the device as tested.

SURFACE POTENTIAL AND CHARGE STORAGE CAPACITY

Having determined the CCD oxide parameters given in Table 3-1, the surface potential versus gate voltage relationships may be calculated for the 8585 Lot 4 devices. The relationship between the surface potential ψ_s, stored charge Q_p, and applied gate voltage V_G is

$$\psi_s = V + V_O - V_O \left(1 + \frac{2V}{V_O}\right)^{\frac{1}{2}} \tag{3-4}$$

where $V = V_G - V_{FB} + \frac{Q_p}{C_{OX}}$ (3-5)

and $V_O = -\epsilon_s q N_D / C_{OX}^2$. (3-6)

C_{OX} is the oxide capacitance/unit area appropriate to the gate being considered.

To define nomenclature, Figure 3-6 shows one bit of an overlapping-gate, 4ϕ CCD. Consistent with Figure 3-2, ϕ_1 and ϕ_3 are surface gates and ϕ_2 and ϕ_4 are buried gates. On the 8585 chip, the surface and buried gates are equal in area as shown in Figure 3-6. The surface potentials are shown in Figure 3-6 appropriate to the one-quarter of the clock period during which time the charge is stored beneath the buried ϕ_2 gate. We consider here simple 4ϕ clocking but other clocking modes are possible such as simulated 2ϕ or 4ϕ double-clocking.

The clock voltages applied to the surface gates (ϕ_1, ϕ_3) are V_{G1} and V_{G2} and to the buried gates (ϕ_2, ϕ_4) V_{G3} and V_{G4}. (These are identified in

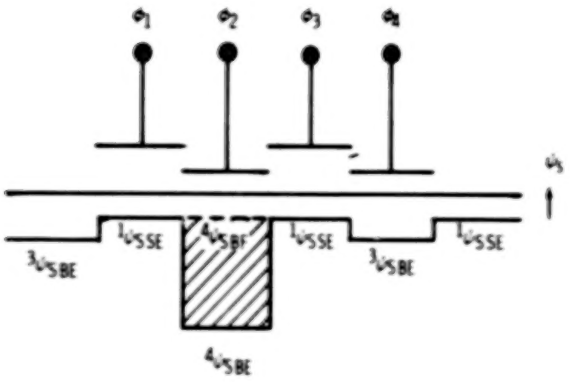

Figure 3-6.- Surface Potentials for One Bit of 4ϕ CCD.

the 20-element CCIRID clock diagram in Section 4, Figure 4-2.) The high or "on" voltages are V_{G2} and V_{G4} with $V_{G2} < V_{G1}$ and $V_{G4} < V_{G3}$*. The surface potential notation used is that the subscripts refer to B = buried gate, S = surface gate, E = empty, F = full, and the superscripts 1, 2, 3, 4 denote the potentials appropriate to clock voltages V_{G1}, V_{G2}, V_{G3}, and V_{G4} respectively.

Referring to Figure 3-6, the ϕ_2 gate is on (clock voltage V_{G4}) and the other three gates are clocked off. ϕ_1 and ϕ_3 are therefore at their off surface potential $^1\psi_{SSE}$ and are empty. The buried gate ϕ_4 is also empty, at potential $^3\psi_{SBE}$. When no charge is being transferred in the CCD, the potential under ϕ_2 is $^4\psi_{SBE}$. The criterion for maximum charge storage in the CCD is evident from Figure 3-6 and occurs when

$$^4\psi_{SBF} = {}^1\psi_{SSE} \tag{3-7}$$

Any less-negative surface potential under gate ϕ_2 resulting from additional charge stored will clearly produce spillover across the ϕ_1 and ϕ_3 gates. The maximum charge that can be stored under ϕ_2 is therefore

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*Signs and notation appropriate to a p-channel CCD are used throughout. When considering the inequalities, recall that gate voltages and surface potentials are negative for a p-channel device in normal operation.

$$Q_{pB\ (max)} \cong C_{OXB}\left({}^{4}\psi_{SBF} - {}^{4}\psi_{SBE}\right)$$

$$\cong C_{OXB}\left({}^{1}\psi_{SSE} - {}^{4}\psi_{SBE}\right) \qquad (3\text{-}8)$$

Considering in a similar manner the fraction of the clock period during which the charge is stored beneath a surface gate (e.g., ϕ_3) one obtains for the maximum charge storage

$$Q_{pS\ (max)} \cong C_{OXS}\left({}^{2}\psi_{SSF} - {}^{2}\psi_{SSE}\right)$$

$$\cong C_{OXS}\left({}^{3}\psi_{SBE} - {}^{2}\psi_{SSE}\right) \qquad (3\text{-}9)$$

Equations (3-8) and (3-9) show that the charge storage capacity may be estimated for a given set of clock voltages from the empty-well surface potentials of the buried and surface gates. Using equations (3-4) through (3-6), with $Q_p = 0$, the ψ_S versus V_G curves appropriate to 8585 Lot 4 were calculated and are plotted in Figure 3-7. These curves give the surface potential beneath the gate when empty for any applied V_G.

A further criterion for simple 4ϕ clocking and for the case of equal gate area is

$$Q_{pB\ (max)} = Q_{pS\ (max)} \qquad (3\text{-}10)$$

which using (3-8) and (3-9) leads to

$${}^{4}\psi_{SBE} = {}^{2}\psi_{SSE}\left(\frac{C_{OXS}}{C_{OXB}}\right) \qquad (3\text{-}11)$$

where ${}^{1}\psi_{SSE} \cong {}^{3}\psi_{SBE} \cong 0$. For lot 4, $C_{OXS}/C_{OXB} = 0.57$,

i.e., the buried gate empty-well potential must be 0.57 of the surface gate empty-well potential for the CCD to correctly transfer its maximum charge. This criterion is shown in Figure 3-7 as a set of dashed lines connecting the buried and surface gate ψ_S curves.

The calculated curves of Figure 3-7 are compared to experimentally-determined clock voltages later in this section.

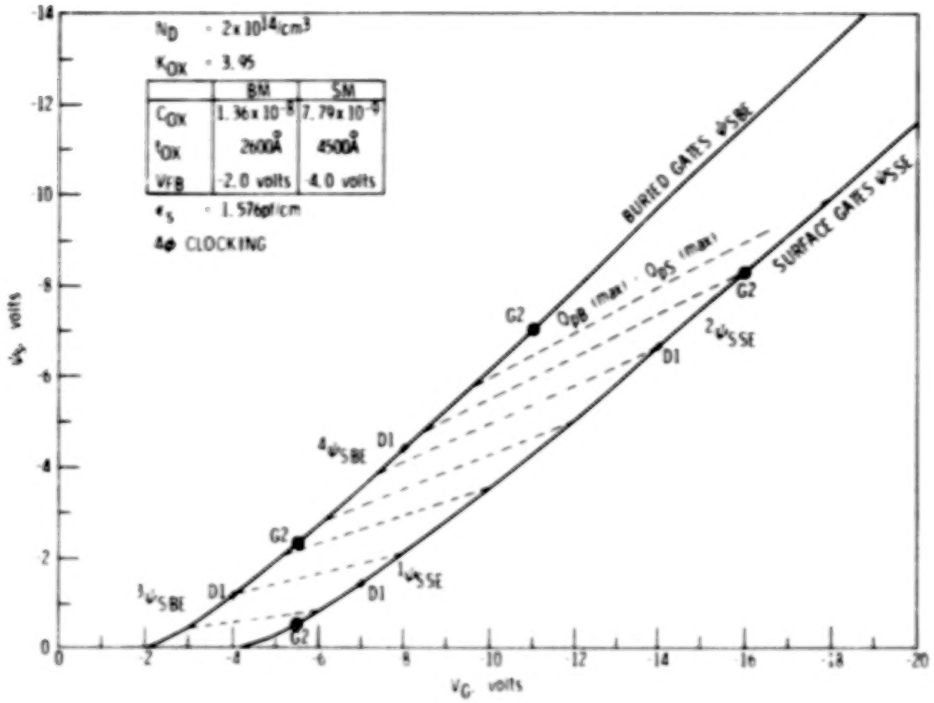


Figure 3-7. - Surface Potential versus Gate Voltage for 8585 Lot 4.

CHANNEL STOP METAL BIAS REQUIREMENTS

Both the two-element and 20-element devices were evaluated using the floating diffusion output circuit shown previously in Figure 3-2. To use this type of circuit successfully, the output p-n junction must have sufficiently low leakage so as not to discharge the output node capacitance once it has been preset to its reference level V_{REF}. The combination of planar InSb p^+-n junctions of good quality which result from the Be ion implantation procedure, along with gate control of surface potential around the junction perimeter, allows this requirement to be met.

In the 8585 mask design, a channel stop metal level is incorporated in the CCD structure which overlaps three of the four sides of the input and output p-n junctions. The channel stop metal serves the combined functions of charge confinement within the CCD channel and junction leakage optimization through gate-controlled diode action. For both effective channel-stopping and optimum junction characteristics, a near-zero surface potential is

required (i. e. , flatband conditions) at the channel edges and around the perimeter of the p-n junctions. Since the n-type side of the p-n junctions is lightly-doped, oxide charge in the gate oxide can readily produce non-zero surface potentials, either accumulating or depleting (or in the extreme case, inverting) the n-region, depending on the sign of the charge. Such surface conditions can markedly affect diode leakage characteristics in a material such as InSb. Applying bias to the channel stop metal of appropriate polarity to balance the oxide charge will restore flatband conditions to the n-region and optimize junction leakage and breakdown.

Analysis of the forward and reverse current-voltage characteristics of the implanted Be junctions in InSb has shown[5] that, at 77 K, the leakage is dominated by generation-recombination current at small bias voltages. For reverse bias voltages (V_R) in excess of approximately 1 volt, the reverse current I_R departs from the $I_R \propto V_R^{\frac{1}{2}}$ dependence expected for G-R current, and instead enters a "soft" breakdown region where the current increases as a superlinear function of V_R. Current in the soft breakdown region arises from both tunneling and avalanche mechanisms for the substrate impurity concentration range of interest and, as such, is quite sensitive to any local enhancement in electric field. For example, the electric field may be increased relative to that associated with the ideal plane (not planar) junction depletion region by junction curvature effects, material defects and inhomogeneities, and non-ideal surface conditions. The soft breakdown region spans several volts and is the region of interest here since junction biases exceed 1 volt for many CCD device requirements, including the output junction.

The soft breakdown current in gated InSb junctions is observed to vary with gate bias in a consistent and qualitatively explainable manner. The influence of gate bias on a p^+-n junction is diagrammed in Figure 3-8, showing the three generalized conditions that can be obtained. Figure 3-8(A) shows the extreme case of the n-region inverted, corresponding to a large negative gate voltage. Leakage is increased in this case due to an increased

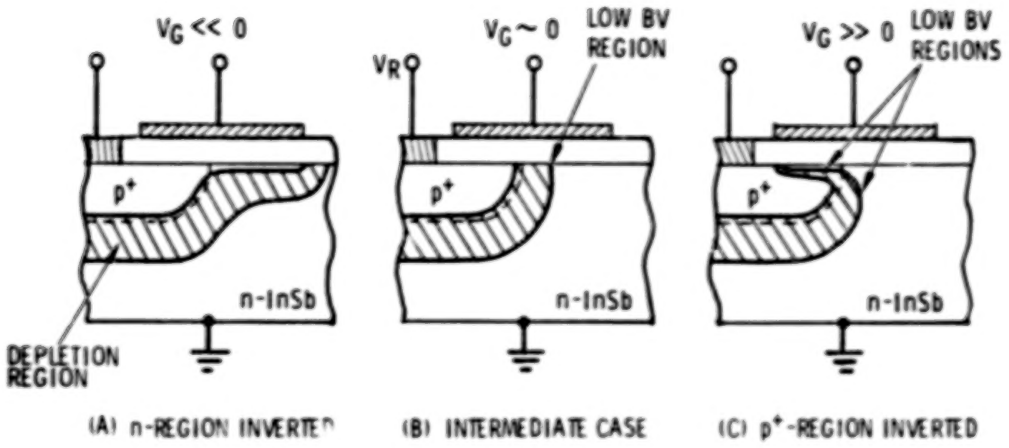


Figure 3-8. - Effect of Surface Conditions on Breakdown Voltage of InSb Planar p-n Junctions.

effective junction area for G-R current generation. Figure 3-8(C) shows the other extreme case of p^+-region inversion corresponding to a large positive gate voltage. The resulting junction depletion regions for both cases are shown in the figure. For p^+-region inversion, case (C), extremely low breakdown voltage (BV) can result due to the high field regions established, identified in the figure. In the absence of a gated structure, conditions identical to (A) and (C) in Figure 3-8 can occur if a large negative or positive Q_{fc} is present in the gate oxide.

As has been shown, Q_{fc} is positive but small in magnitude for the LTCVD SiO_2 - InSb MOS process, so that the extreme inversion cases of Figure 3-8(A) and (C) do not occur. The intermediate case of Figure 3-8(B) is therefore of interest, corresponding to small gate bias or equivalent small oxide charge densities.

The intermediate case surface effect is shown in more detail in Figure 3-9. Band diagrams are also given in this figure corresponding to the bias conditions in the soft breakdown region. In the bulk region away from the surface, the field in the depletion region E_B increases approximately linearly with reverse bias V_R according to the equation given in Figure 3-9(A).

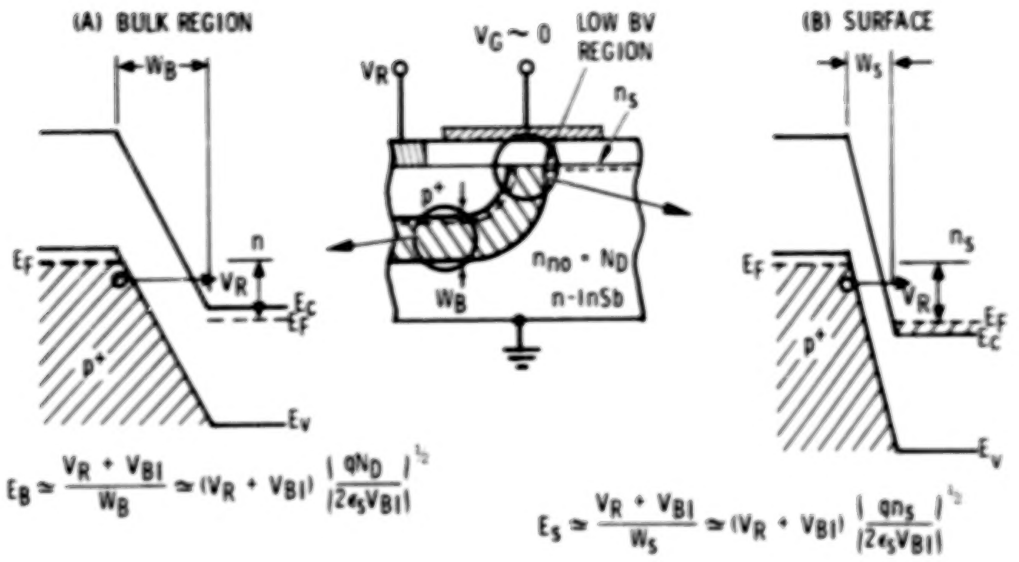


Figure 3-9. - Surface Effect, Intermediate Case.

The higher the base doping N_D, the higher will be the field for a given V_R. As the field E_B increases, additional tunneling of electrons from the p^+ to the n-region occurs as shown in the band diagram of Figure 3-9(A), in addition to increased avalanche current. Bulk-junction dominated breakdown voltages in the absence of surface effects can be up to 10 volts for InSb diodes at 77 K, with appropriate substrate doping. Since the definition of breakdown voltage is arbitrary, the criterion used throughout the program is BV = V_R at I_R = 10 μa, for a junction area of 5×10^{-4} cm^2.

The current in the soft breakdown region can be influenced by surface conditions, however, as shown in Figure 3-9(B). Here a positive Q_{fc} or equivalent positive gate voltage will induce an accumulation layer on the n-side of the junction with surface electron concentration n_s. The field at the surface E_s, therefore, will be higher than in the bulk by the factor $(n_s / N_D)^{\frac{1}{2}}$ for the same applied V_R, and increased breakdown current will flow around the perimeter of the junction at the surface.

Summarizing, the soft breakdown characteristics of InSb planar p^+-n junctions are influenced by the charge Q_{fc} in the gate oxide. The positive

Q_{fc} present in the LTCVD SiO_2 oxide accumulates the lightly-doped n-side of the junction and gives rise to increased breakdown current relative to that of the bulk junction. Negative gate bias restores the optimum surface potential at the surface, and this function is accomplished by the channel stop metal.

Prior to clocking the two-element CCIRIDs, the output circuit was biased up and the optimum channel stop voltage (V_{CS}) determined. The output timing and waveform are shown schematically in Figure 3-10. Since the last clocked gate is ϕ_3, ϕ_{RST} is timed to preset the output node to voltage

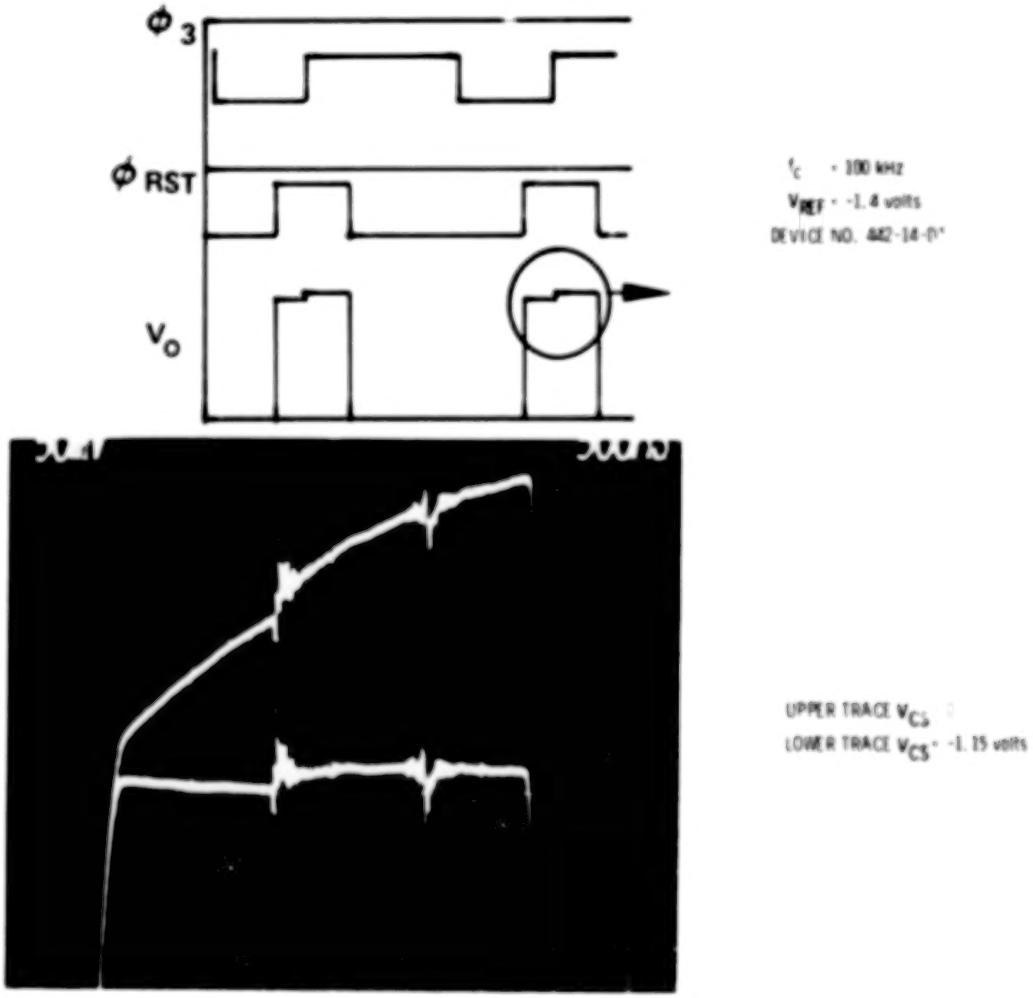


Figure 3-10. - InSb CCD Floating Diffusion Output (Showing Negligible Output Diode Leakage).

V_{REF} slightly in advance of ϕ_3 turning off. When ϕ_3 turns off, charge is transferred across the output gate (at dc level V_{OG}) to the output junction, increasing its potential toward zero. The oscilloscope photograph in Figure 3-10 shows the source-follower output voltage (V_o) during the period of time when the output junction is floating. The upper trace is for the channel stop unbiased, $V_{cs} = 0$; i. e. , no bias has been applied to eliminate the accumulation layer beneath the channel stop metal. This corresponds to the condition in Figure 3-9(B), and the additional leakage current is decreasing the output node voltage toward zero as evident from Figure 3-10. The lower trace in Figure 3-10 shows the elimination of this surface leakage by negative-biasing the channel stop metal to slightly above its flatband voltage. This channel stop bias effect was observed reproducibly on all the InSb CCDs tested during the program.

TWO-ELEMENT InSb CCIRID OPERATION

The shift register of the two-element CCIRID was first operated independently of the detectors by biasing the transfer gate ϕ_T and photogate ϕ_p off, and applying signal pulses to the fat zero input. ϕ_T and ϕ_p were biased to near their respective flatband voltages rather than held at zero so that these gates were not in accumulation.

Figure 3-11 shows the output of device 442-14-G2 with ten signal pulses applied to the FZ input. All clock voltages and test conditions are listed in the figure. Because of the availability of compatible planar p^+-n junctions in InSb, the FZ input structures on the InSb CCIRIDs are similar to conventional Si CCD inputs, and it is not necessary to rely on surface avalanche breakdown or tunneling for signal and FZ charge input. To input the signal charge, the input diode was held at zero volts (i. e. , tied to substrate); the signal pulses were applied to the input buried gate V_{IB}; and the input surface gate V_{sc} was held at a dc potential. When the input buried gate is turned on,

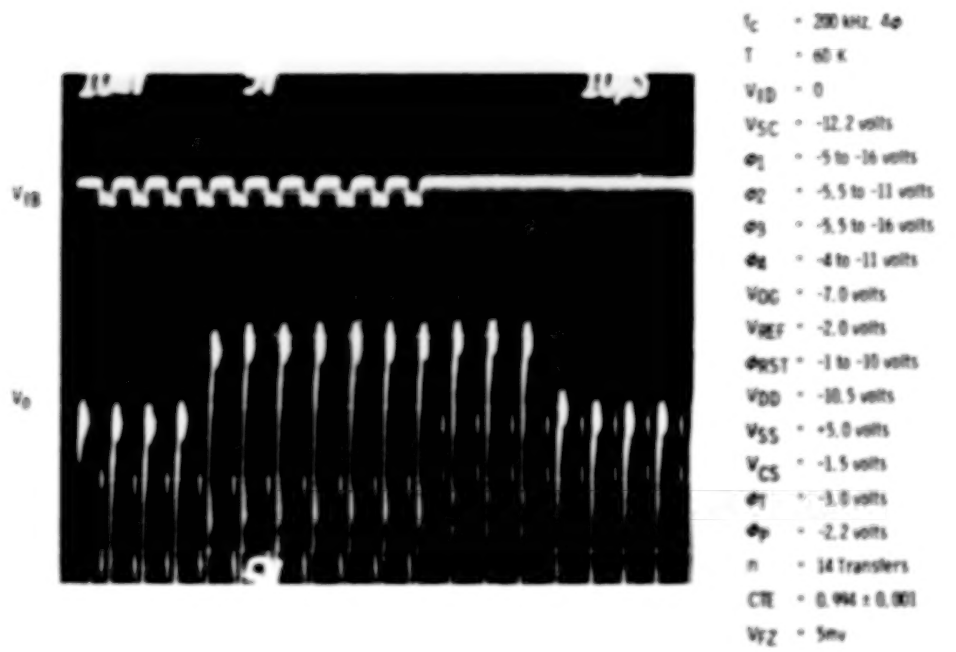

V_{IB}
V_o
f_c = 200 kHz, 4φ
T = 60 K
V_{ID} = 0
V_{SC} = -12.2 volts
ϕ_1 = -5 to -16 volts
ϕ_2 = -5.5 to -11 volts
ϕ_3 = -5.5 to -16 volts
ϕ_R = -4 to -11 volts
V_{OG} = -7.0 volts
V_{REF} = -2.0 volts
ϕ_{RST} = -1 to -10 volts
V_{DD} = -18.5 volts
V_{SS} = +5.0 volts
V_{CS} = -1.5 volts
ϕ_T = -3.0 volts
ϕ_p = -2.2 volts
n = 14 transfers
CTE = 0.994 ± 0.001
V_{FZ} = 5mv

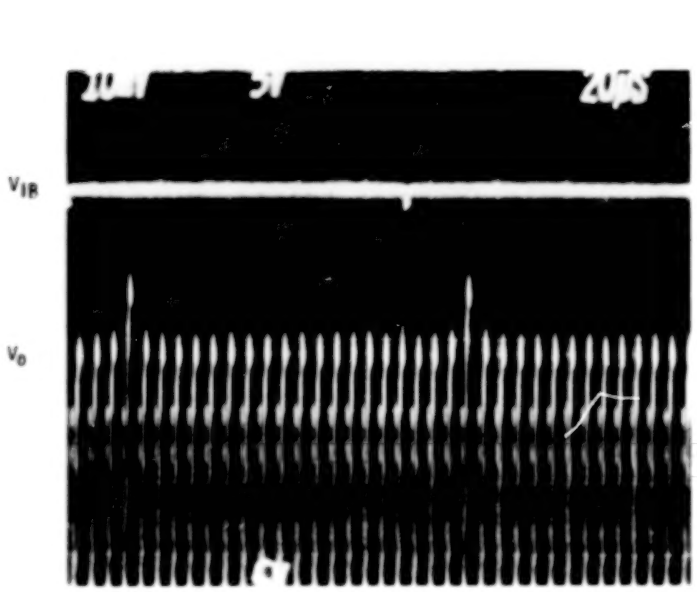
Figure 3-11. - Output of Two-Element ($3\frac{1}{2}$ Bit) InSb CCIRID with Ten Input Pulses (Device No. 442-14-G2).

the first clocked gate (ϕ_2) is off*, and the input p^+ region supplies holes to the well beneath the input surface gate. The input buried gate was turned off, and ϕ_2 turned on to complete the input cycle. The input structures on the 8585 devices are also capable of being clocked in a fill-and-spill sequence, which gives superior control over input charge; however, due to other priorities this was not investigated during this program.

The upper trace in Figure 3-11 shows the signal pulses applied to V_{IB} and the lower trace the source follower output voltage V_o. In this and all other oscilloscope photographs of the CCD outputs in this report, V_o is shown without further amplification, filtering, or sample-and-hold. The output in Figure 3-11 is correctly delayed by $3\frac{1}{2}$ clock periods. CTE was calculated using the usual measurement of trailers and loss in the leaders. For the multiple pulse train of Figure 3-11, the CTE obtained was 0.994 ± 0.001.

*For the case described here, the pulse applied to V_{IB} leads clock ϕ_2 and does not overlap it. Charge was also input with the V_{IB} pulse in phase with ϕ_2.

Figure 3-12 shows the output of the same device with a single pulse applied to the FZ input. Measurement of CTE from Figure 3-12 yielded CTE = 0.996 ± 0.0003.



f_c = 200 kHz, 4ϕ
T = 60 K
V_{ID} = 0
V_{SC} = -11.9 volts
ϕ_1 = -6 to -16 volts
ϕ_2 = -5 to -11 volts
ϕ_3 = -5.5 to -16 volts
ϕ_4 = -3 to -10.5 volts
V_{OG} = -6.7 volts
V_{REF} = -2.0 volts
ϕ_{RST} = -1 to -10 volts
V_{DD} = -10.5 volts
V_{SS} = +5.0 volts
V_{CS} = -1.5 volts
ϕ_T = -3.0 volts
ϕ_p = -2.2 volts
n = 14 Transfers
CTE = 0.996 ± 0.0003
V_{FZ} = 5mv

Figure 3-12. - Output of Two-Element ($3\frac{1}{2}$ Bit) InSb CCIRID with Single Input Pulse (Device No. 442-14-G2).

For reference purposes, the equations used to calculate CTE from the output pulse trains are collected here.

Method 1[6]

For a single charge packet input into the CCD register, the inefficiency per transfer ϵ may be calculated from the relation

$$n\epsilon = B/A \tag{3-12}$$

where n = number of transfers

A = magnitude of principal output

B = magnitude of first trailer

Assuming no charge loss, the efficiency per transfer (CTE) is then

$$CTE = 1 - \epsilon \tag{3-13}$$

Method 2

For multiple charge packets (i.e., pulse train) input into the CCD, if

B' = magnitude of the first output pulse

A' = maximum value of the signal output

then

$$CTE = \left(B'/A'\right)^{1/n} \tag{3-14}$$

A sufficient number of charge packets must be input to determine the true maximum value A'.

Method 3

Again for multiple charge packets, if

δ_j = charge deficits in leaders, normalized to maximum signal output

δ_j' = charge in trailers, normalized to maximum signal output

and denoting the sums of the normalized charge deficits and trailers as

$$S_L = \sum \delta_j$$

$$S_T = \sum \delta_j'$$

then it can be shown that

$$S_L = S_T \cong (CTE)^n \left[\frac{n\epsilon}{(1-\epsilon)^{n+1}}\right]$$

$$\cong \frac{n\epsilon\ (1-\epsilon)^n}{(1-\epsilon)^{n+1}}$$

$$\cong \frac{n\epsilon}{1-\epsilon} \tag{3-15}$$

Solving for ϵ:

$$\epsilon \cong \frac{S_L}{S_L + n} \cong \frac{S_T}{S_T + n} \tag{3-16}$$

The charge transfer efficiency and the dominant mechanisms affecting it are discussed in greater detail in the Discussion of Test Results, Section 5. Figures 3-11 and 3-12 are representative of the two-element devices tested. Figures 3-13 and 3-14 show FZ input-output transfer characteristics for another two-element CCIRID, No. 442-14-D1. The optimum CTE for these devices was obtained with a 10 to 15% FZ charge.

The observed clock voltages are in reasonable agreement with the calculated surface potential versus gate voltage diagram, Figure 3-7. The empty-well surface potentials corresponding to the clock voltages of Figure 3-13, device 442-14-D1, for example, are plotted on the ψ_{SBE} and ψ_{SSE} curves in Figure 3-7 and labelled "D1." The -4 to -8 volt clocks on ϕ_2 and ϕ_4 swing the surface potential (ψ_{SBE}) from about -1 to -4.4 volts. The clock voltages on the surface gates, -7 to -14 volts, swing ψ_{SSE} from -1.4 to -6.7 volts. The criterion for equal surface- and buried-gate charge capacity expressed by equation (3-11) is seen to be closely satisfied.

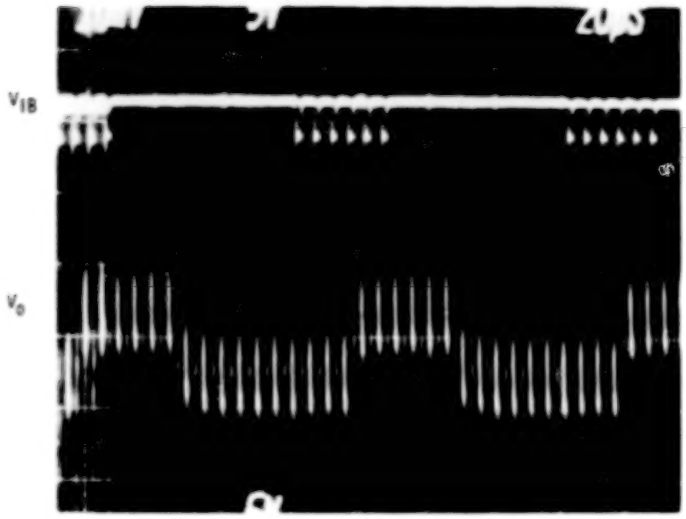
Under the clock conditions of Figure 3-13, the CCD should be capable of transferring a maximum charge calculated from equation (3-9):

$$Q_{pS}\ (\max) = (7.79 \times 10^{-9})\ (-1.2 + 6.7)$$

$$= 2.67 \times 10^{11}\ \text{holes/cm}^2$$

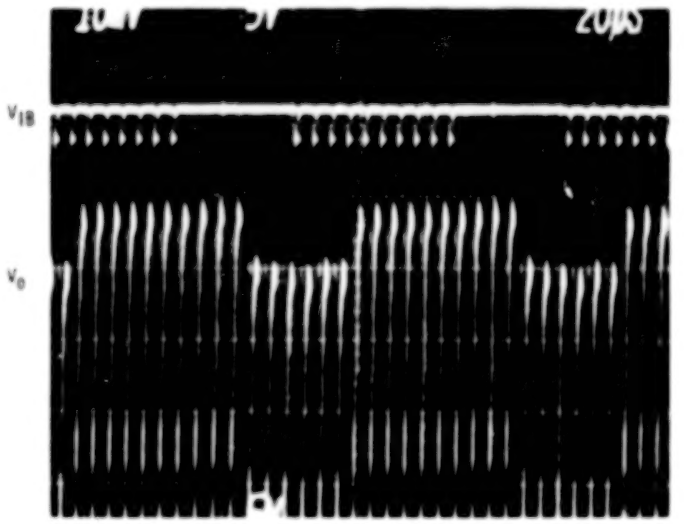
The storage area of the two-element CCD is 0.4×4 mils $= 1.03 \times 10^{-5}$ cm^2 giving a charge capacity of 2.75×10^6 holes.

Considering in a similar manner the clock voltages of Figure 3-11 (Device No. 442-14-G2), the empty-well surface potentials are also plotted in Figure 3-7 (points "G2"). The balance between ${}^4\psi_{SBE}$ and ${}^2\psi_{SSE}$ in this case is not as close as for device D1. The maximum charge capacity for these conditions is



f_c = 200 kHz, 4φ
T = 63 K
V_{ID} = 0
V_{SC} = -12 volts
ϕ_1 = -7 to -14 volts
ϕ_2 = -4 to -8 volts
ϕ_3 = -7 to -14 volts
ϕ_4 = -4 to -8 volts
V_{OG} = -7.5 volts
V_{REF} = -1.5 volts
ϕ_{RST} = -1 to -10 volts
V_{DD} = -10.5 volts
V_{SS} = +5.0 volts
V_{CS} = -1.0 volt
ϕ_T = -4.7 volts
ϕ_p = -0.2 volt

Figure 3-13. - Output of Two-Element ($3\frac{1}{2}$ Bit) InSb CCIRID No. 442-14-D1 with Six Input Pulses.



f_c = 200 kHz, 4φ
T = 54 K
V_{ID} = 0
V_{SC} = -13.3 volts
ϕ_1 = -8 to -16 volts
ϕ_2 = -4 to -7.2 volts
ϕ_3 = -7 to -15 volts
ϕ_4 = -4.8 to -8 volts
V_{OG} = -8.0 volts
V_{REF} = -2.0 volts
ϕ_{RST} = -1 to -10 volts
V_{DD} = -10.5 volts
V_{SS} = +5.0 volts
V_{CS} = -1.55 volts
ϕ_T = -4.7 volts
ϕ_p = -0.2 volt

Figure 3-14. - Output of Two-Element ($3\frac{1}{2}$ Bit) InSb CCIRID No. 442-14-D1 with Ten Input Pulses.

$$Q_{pS}\ (\text{max}) = (7.79 \times 10^{-9})\ (-2.3 + 8.3)$$

$$= 2.91 \times 10^{11}\ \text{holes/cm}^2$$

which multiplying by the gate area is 3.0×10^6 holes, close to the previous result.

To determine from the output voltage the actual charge being transferred in the CCD, the output node capacitance must be known. In Section 4, the output capacitance (C_o) of the 20-element arrays (using the off-chip 3N163 MOSFETs) is calculated to be approximately 6pf. C_o for the two-element arrays was higher, due to a difference in wirebonding arrangement that was used earlier in the program. For the two-element arrays, the output diode pad was first connected by a wirebond to a spare (floating) lead of the flatpack; two additional wirebonds connected the floating flatpack lead to the appropriate pads of the two 3N163 MOSFETs. Additional output capacitance resulted from the flatpack lead-to-ground and flatpack socket/pin-to-ground capacitances.

Of several ways to infer C_o, it was estimated for the two-element arrays by observing the dependence of the output on the output gate voltage V_{OG}. With device No. 442-14-G2 transferring charge under the conditions of Figure 3-11, and keeping V_{REF} constant at -2 volts, V_{OG} was increased (more negative) until the output signal voltage V_s went to zero. This was observed to occur at $V_{OG} = -9$ volts. From the ψ_{SBE} curve of Figure 3-7 (the output gate is a buried gate), $\psi_{OG} = -5.3$ volts at $V_{OG} = -9$ volts. Under this condition, the signal charge being transferred by the CCD to the output is held under V_{OG} and does not reach the output diode. The charge magnitude is

$$Q_p\ (OG) = C_{OXB}\ (-2 + 5.3)$$

$$= 4.5 \times 10^{-8}\ \text{coulombs/cm}^2$$

The area of the output gate is approximately one-fourth that of the ϕ_1 - ϕ_4 gates (the channel width under the output gate is narrowed to the width of the output diode, see Figure 3-1). Its area is 2.6×10^{-6} cm^2, giving Q_p (OG) $\times$ $A_{OG} = 1.2 \times 10^{-13}$ coulombs. This quantity of charge with V_{OG} decreased so as to effect total transfer to the output diode gives an output signal voltage (Figure 3-11) $V_s = 11$ mv. The output voltage is related to the charge by

$$V_s = (0.9) \frac{Q_s}{C_o} \tag{3-17}$$

where the factor 0.9 approximates the product of the 3N163 source-follower gain and the "unity-gain" buffer amplifier. Solving for C_o with $Q_s = 1.2 \times 10^{-13}$ coul yields $C_o \cong 10$ pf, a reasonable value considering the basic 6pf capacitance plus the additional capacitance associated with the flatpack and socket.

Using this value of C_o, the maximum charge capacity of the CCD operating under the conditions of Figure 3-11 therefore corresponds to a maximum total output voltage ($V_s + V_{FZ}$) equal to:

$$V_o = \frac{q\,(0.9)\,(3 \times 10^6)}{10 \times 10^{-12}} = 43 \text{ mv}$$

Care was taken in testing to always introduce FZ plus signal charge levels such that the total output voltage level V_o was less than the observed output saturation voltage. This was to ensure that the true peak amplitude heights relative to the leaders and trailers were obtained, so avoiding false CTE readings. However, even taking this into account the total output voltage magnitudes observed, with the input gate and clock voltages adjusted for optimum CTE, were consistently lower than the 43 mv calculated above. This result has been found by analysis of the input gate voltages recorded during testing to be due to the FZ input circuit supplying smaller charge packets than the CCD is capable of transferring. For the input gate conditions of Figure 3-11, the total input charge (FZ + signal) was calculated to be 2.1×10^{-13} coul or 1.3×10^6 holes, less than one-half of the calculated

CCD capacity of 3×10^6 holes. The expected output voltage for this charge input is

$$V_o = \frac{(0.9)(2.1 \times 10^{-13})}{10 \times 10^{-12}} = 18.9 \text{ mv}$$

The observed total output voltage was $V_{FZ} + V_s = 5 + 11$ mv = 16 mv, in reasonable agreement with the calculation. $V_{FZ} = 5$mv was found experimentally to be the typical FZ level required to maximize CTE. It represents approximately 12% of the CCD charge capacity.

Further evidence that the input circuit was limiting the two-element output voltage magnitudes in Figures 3-11 through 3-14 was provided by the facts that: (1) larger (30-mv) output voltage swings were obtained when adjusting clock and input voltage parameters for maximum output amplitude but neglecting CTE; and (2) an output voltage of 25 mv was observed with the photogates biased and viewing an infrared flux, with the CCD clocks ϕ_1 - ϕ_4 set at the same voltages which gave the smaller output levels when inputting with the FZ gates.

Figure 3-15 shows the larger output level observed for device No. 442-14-G2 when the parameters were adjusted to peak V_o rather than optimize CTE. V_{FZ} = and $V_o = V_s = 30$ mv. Comparing the parameters of Figure 3-15 to those of Figures 3-11 and 3-12 reveals that the only significant change was an increase in the low level of ϕ_1 and ϕ_3 from approximately -5.5 to -8 volts, with high levels remaining at -16 volts. This increases the off surface potential ($^1\psi_{SSE}$) under ϕ_1 and ϕ_3 from -0.5 to -2.1 volts. (Figure 3-7). This change simultaneously results in increased charge storage in the CCD and an increased quantity of charge introduced by the input circuit. The calculated maximum charge capacity increases from 3×10^6 to 3.9×10^6 holes. This occurs because some additional charge can be stored under the surface gates on either side of the buried gate which is clocked "high." (This represents an intermediate condition between conventional 4ϕ clocking and "double clocking"). More charge is introduced at the FZ input because under this clock condition the first ϕ_3 gate, in addition to the first ϕ_2

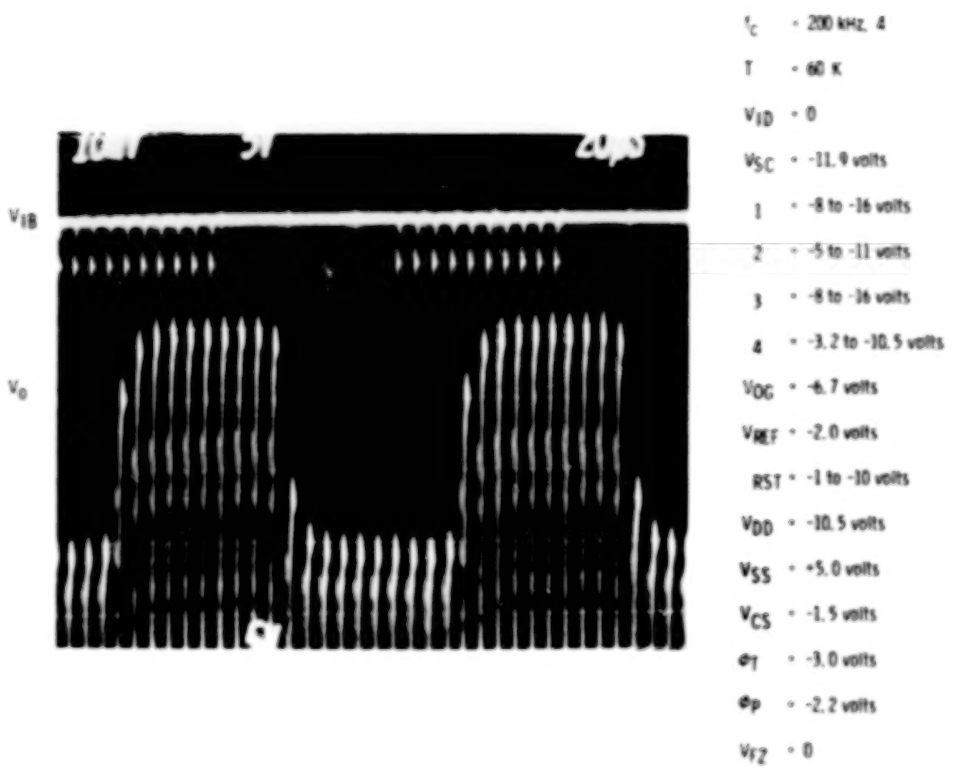

V_{IB}
V_o
f_c = 200 kHz, 4
T = 60 K
V_{ID} = 0
V_{SC} = -11.9 volts
1 = -8 to -16 volts
2 = -5 to -11 volts
3 = -8 to -16 volts
4 = -3.2 to -10.5 volts
V_{OG} = -6.7 volts
V_{RGT} = -2.0 volts
RST = -1 to -10 volts
V_{DD} = -10.5 volts
V_{SS} = +5.0 volts
V_{CS} = -1.5 volts
ϕ_T = -3.0 volts
ϕ_P = -2.2 volts
V_{FZ} = 0

Figure 3-15. - Output of Two-Element ($3\frac{1}{2}$ Bit) InSb CCIRID No. 442-14-G2 without Fat Zero and with Parameters Adjusted for Maximum Output Voltage.

gate, fills to a 2-volt level when V_{IB} is turned on. This adds a quantity of input charge equal to 1.2×10^{-13} coul, giving a calculated total output voltage in this case of

$$V_o = \frac{(0.9)\,(2.1 \times 10^{-13} + 1.2 \times 10^{-13})}{10 \times 10^{-12}} = 29.7 \text{ mv}$$

in good agreement with the observed output magnitude in Figure 3-15. The CTE is lower for this set of clock conditions, approximately 0.98.

More testing is needed, in particular studying in detail the change in CCD output with variations in each input gate voltage level, to quantify and improve the input circuit operation. In particular, fill-and-spill and other input circuit clocking methods must be investigated. The basic operability of the two-element shift register that was verified, however, served the purpose for which it was intended, that is, a stepping-stone to the larger

20-element CCIRID. The device demonstrated for the first time compatibility among the implanted diode, LTCVD SiO_2, and sputtered Al/SiO_2 processes. As has been described in this section, the clock voltages were close to expected values (Figure 3-7), and the output voltage levels were consistent with a 10 pf output capacitance and the calculated input charge levels. In these tests, however, it is believed that the register was not operated up to its maximum charge capacity.

The operation of the two-element CCDs was not evaluated over a wide range of clock frequency. One device, No. 442-14-D1, was operated at f_c = 1 MHz and T = 80 K. The CTE measured at this clock frequency was 0.992 ± 0.001.

One of the two-element CCIRIDs, No. 442-14-D1, was operated in the optical mode. The output is shown in Figure 3-16. The top trace is the photogate clock, and the trace below it the transfer gate. The period of the transfer gate pulse, in this case 300 μsec, determines the integration time (T_{int}). The CCIRID was viewing an 800 K blackbody through a cold 2.65-μm spike filter (photon flux calculations for the dewar and filter used are given in Section 4). The uppermost output waveform is for the blackbody aperture blocked; below it, with the IR flux incident on the CCIRID. When illuminated, the output shows a 16-mv signal, a zero, and then a 10-mv signal pulse. The signal pulses are from the detectors nearest and farthest from the output, respectively, and the zero between them arises from the isolation bit.

Since the transfer gate may be clocked independently of the CCD clocks, the integration time may be set up for any of three conditions: (1) $T_{INT} = N_B T_C$ (the condition for repetitive multiplexing) where N_B is the number of CCD bits/line; (2) $T_{INT} > N_B T_C$ (integration time exceeds line readout time); and (3) $T_{INT} = T_C$ (TDI). The range of useful integration times under a given set of test conditions depends on the sum of background and signal photon flux; the device storage capacity; and competing dark current processes.

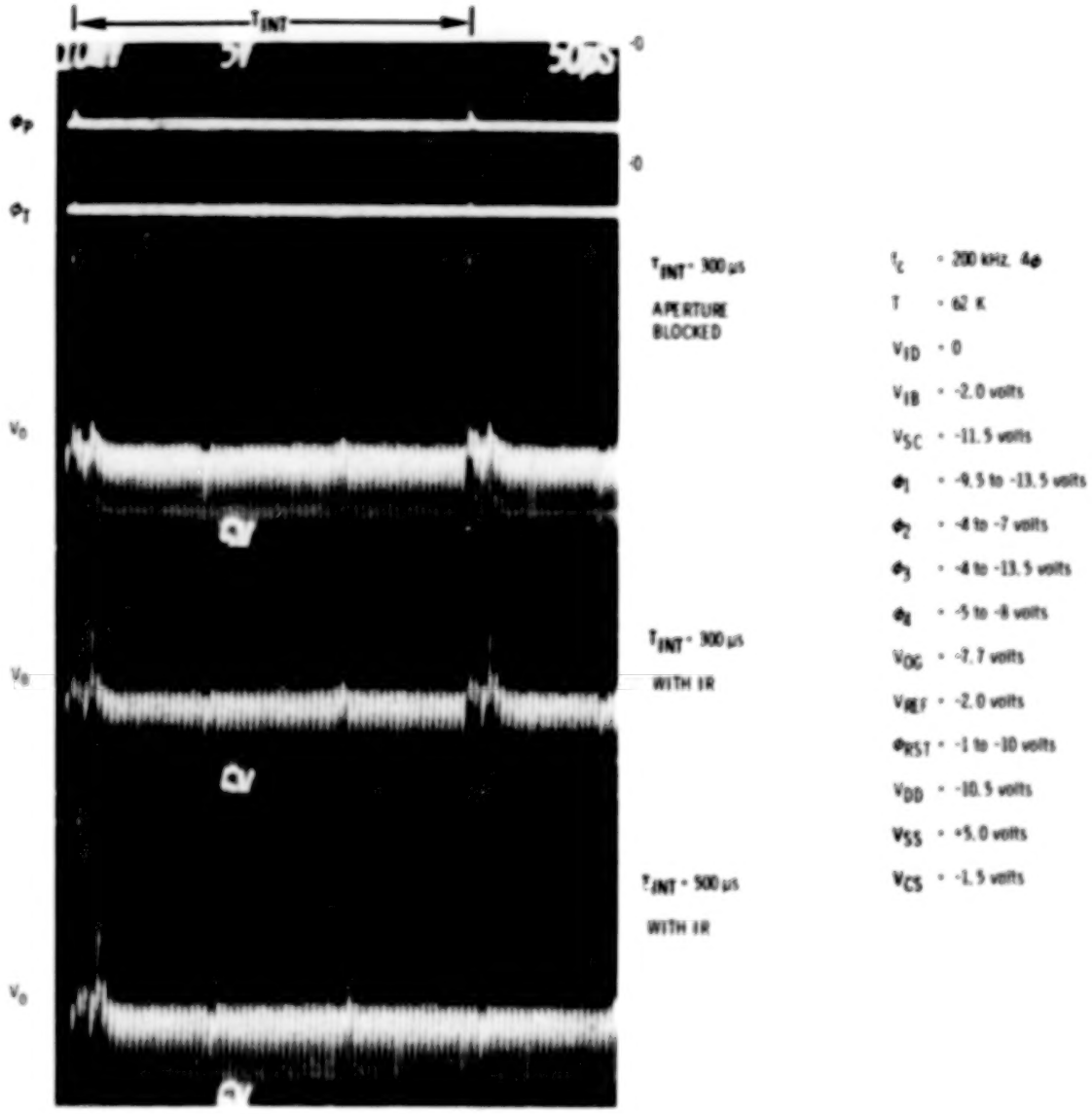


Figure 3-16. - Two-Element InSb CCIRID No. 442-14-D1 Operating in Optical Mode, Array Viewing 800 K Blackbody through 2.65-μm Spike Filter.

Because the two-element CCIRID is short ($N_B = 3$)*, and the signal (and background) photon flux levels resulting from the narrow-band spike filter were low, an integration time longer than $3T_C$ was necessary to achieve measurable signal output levels, i.e., condition (2) above was used rather than the repetitive multiplexing condition (1). In Figure 3-16, the top and middle output waveforms are for $T_{INT} = 60\,T_C = 300\ \mu sec$, and the lower output for $T_{INT} = 100\,T_C = 500\ \mu sec$. Alternatively, T_C could be increased to achieve any desirable T_{INT} for a given N_B. The general testing approach used in this phase of the program was to set up and optimize clocks and biases for a given f_c (using the FZ input), and then maintain this constant f_c while increasing integration time ($T_{INT} > N_B T_C$).

The reduced amplitude of the second detector output seen in Figure 3-16, which at first might be ascribed to transfer inefficiency, is believed to be due to a defective (low-resistance) photogate with only a small contribution from transfer loss. A processing problem led to a high incidence of shorted or low-resistance photogates on both the two-element and 20-element devices processed during this program. The identification of this problem and its proposed solution is discussed in Section 5. A considerably smaller reduction in the second detector output would result from transfer loss with the CTEs measured for the two-element CCIRIDs. Taking a conservative value of CTE = 0.990, the relative magnitudes of the first and second outputs should be $(0.99)^4$ and $(0.99)^{12}$, respectively, since the detector charges undergo 4 and 12 transfers to reach the output. The second detector output signal should therefore be 0.922 of the first, compared to the observed ratio of 0.625 for $T_{INT} = 300\ \mu sec$. Even a CTE as low as 0.98 only reduces the second detector output to 0.851 of the first. Further evidence of a defective photogate is that the ratio of the second to the first output does not remain constant as the signal is increased, as seen in the bottom output trace of

*There are 3 bits from detector 1 to the output but $3\frac{1}{2}$ bits from the FZ input to the output. A similar situation holds for the 20-element CCIRID: there are 20 bits from detector 1 to the output; $20\frac{1}{2}$ bits from FZ input to the output.

Figure 3-16. The second output saturates at 10 mv, while the first output continues to increase.

Further evaluation of the two-element CCIRIDs was not carried out, since 20-element devices from another wafer lot became available for evaluation at this point. With the smaller two-element CCIRIDs, however, the first proof of the improved fabrication process was obtained along with the first demonstration of readout of InSb MOS detectors with an InSb CCD shift register.

Section 4

20-ELEMENT InSb CCIRID

DEVICE DESCRIPTION

The design and fabrication of the 20-element InSb CCIRIDs have already been discussed in Section 2. Figure 2-5 and Table 2-3 provided the details of the 4Φ, overlapping gate CCD structure and the process sequence for the 20-element arrays, respectively. For reference purposes, Table 4-1 summarizes the nominal design and process parameters for the device. Each device component, e.g., starting material, photogates, channel stop, etc., has been discussed in greater detail in the previous sections. Figure 4-1 is a photomicrograph of a 20-element CCIRID after completion of processing. The dark squares are the photogate detectors; directly above them in the photograph is the CCD channel. Considerable chip area in this developmental device is taken up by clock bus lines and bonding pads. This would not be the case for an area CCIRID array, the architecture of which would be designed to minimize the ratio of clock line and pad area to active (detector plus CCD channel) area.

Table 4-1.- Nominal Design and Process Parameters for 20-Element InSb CCIRID

DETECTORS	MOS PHOTOGATES
DETECTOR SIZE	35μm x 32.5μm
DETECTOR SPACING	50μm
CCD DESIGN	4Φ p-CHANNEL
NUMBER OF CCD BITS	20½
CCD GATE LENGTH	12.5μm
CHANNEL WIDTH	105μm
SUBSTRATES	n-TYPE CZ InSb, $N_D \leq 2 \times 10^{14}/cm^3$
GATE OXIDE	1000 Å LTCVD SiO_2
OXIDE THICKNESS, BURIED METAL	2500 Å
OXIDE THICKNESS, SURF METAL	4500 Å
CCD STORAGE CAPACITY	5×10^6 CARRIERS
CHANNEL STOP	BIASED FIELD PLATE
ON-CHIP JUNCTIONS	Be-IMPLANTED p^+-n
OUTPUT	FLOATING DIFFUSION
OUTPUT CAPACITANCE	
OUTPUT JUNCTION	0.3 pf
MOSFET INPUT	1.9 pf
STRAY	3.9 pf
TOTAL	6.1 pf

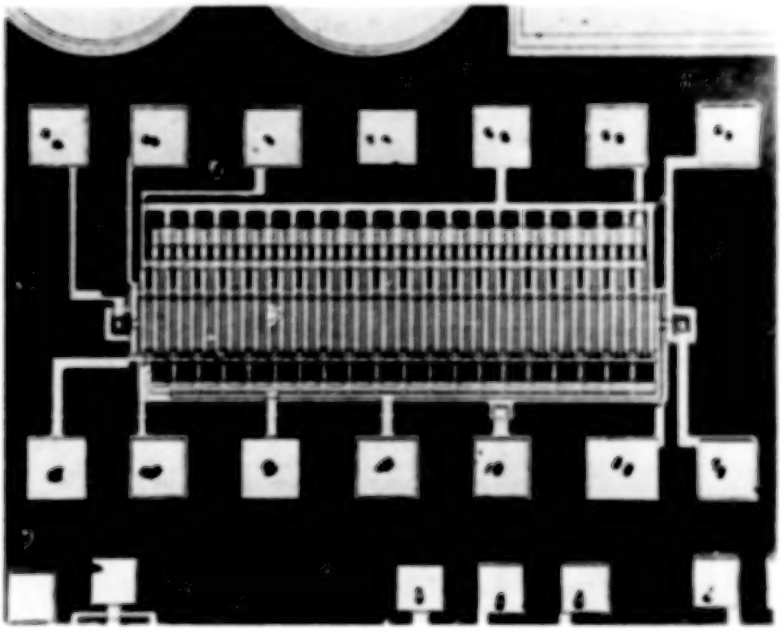


Figure 4-1. - 20-Element InSb CCIRID.

The schematic diagram for the 20-element array is identical to the two-element device and was shown in Figure 3-2 of the previous section. There are 82 clocked gates in the shift register (20 1/2-bits) and, similar to the two-element device, the first clocked gate is ϕ_2 and the last clocked gate is ϕ_3. Input and output circuit gates and nomenclature are also identical.

Figure 4-2 gives the timing diagram for the 20-element CCIRID, with the photogate and transfer gate periods shown as required for the detector multiplexing mode $T_{INT} = N_B T_C$. On the right-hand side of Figure 4-2, the voltage levels are identified as they are referred to in the text.

Beginning with ϕ_1 through ϕ_4, these are the shift register clocks appropriate to a 4ϕ CCD. The "on" time of the clocks (i.e., at voltages V_{G2} and V_{G4}) may be varied from $T_C/4$ (simple four-phase clocking) to $T_C/2$ (4ϕ double clocking); the latter is illustrated in Figure 4-2. Finite fall time on the ϕ_1 though ϕ_4 clocks is also shown in Figure 4-2; although a detailed study was not carried out in the program, some amount of fall time (typically $T_C/8$) was observed to optimize device performance.

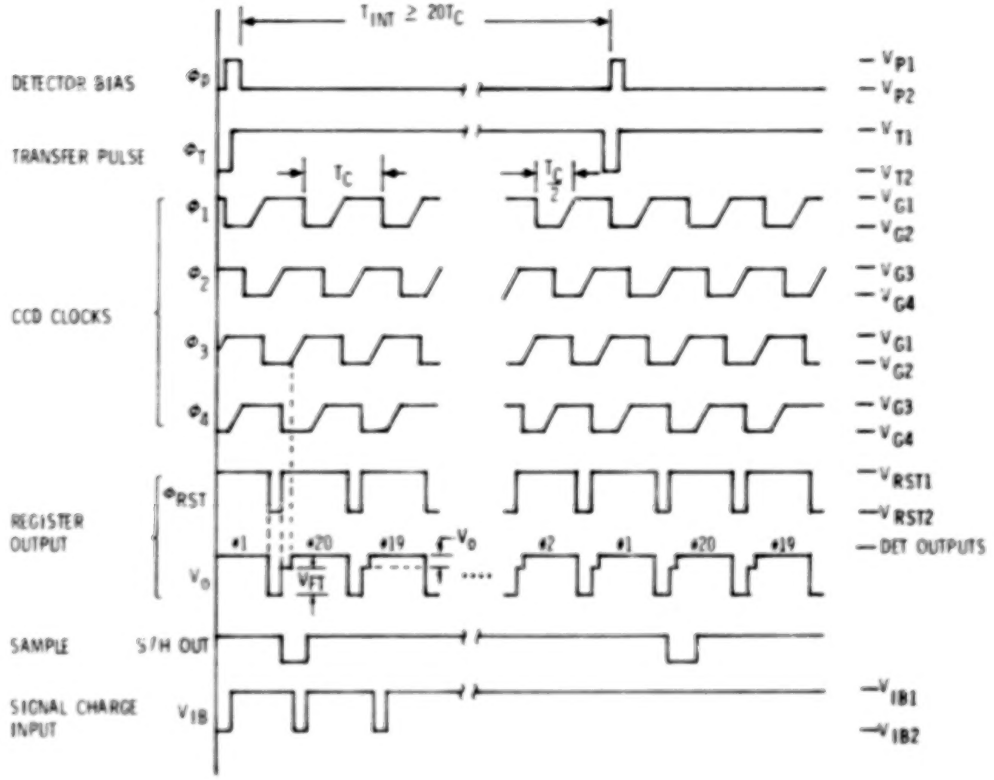


Figure 4-2. - 20-Element CCIRID Timing Diagram (For Detector Multiplexing Mode $T_{INT} \geq N_B T_C$).

The output circuit voltages are V_{OG}, Φ_{RST}, V_{REF}, V_{DD}, and V_{SS}. All are dc except for Φ_{RST}, the clock on the gate of the reset MOSFET; its timing is shown below Φ_4 in Figure 4-2. During the time that the last clocked gate Φ_3 is at its on voltage V_{G2}, Φ_{RST} is switched to $V_{RST2} = -10$ volts. This turns the reset transistor on and presets the output diode to voltage V_{REF}. Just prior to Φ_3 being lowered to its off voltage V_{G1}, the reset transistor is turned off by switching Φ_{RST} from V_{RST2} to $V_{RST1} = -1$ volt, which leaves the output node floating. As Φ_3 goes low, whatever charge it contained is pushed out of the Φ_3 well, across the V_{OG} gate, into the output diode potential well. The resulting output voltage V_o is shown schematically in Figure 4-2, below Φ_{RST}.

When Φ_{RST} is switched from V_{RST2} to V_{RST1} and vice versa, a parasitic feedthrough voltage results at the output, identified as V_{FT} in Figure 4-2. The CCD output signal V_o rides on this feedthrough pedestal as

shown in the figure. The feedthrough voltage V_{FT} is directly proportional to the gate-to-source capacitance (C_{gs}) of the reset transistor. For the discrete 3N163 MOSFET, C_{gs} = 0.7 pf resulting in a relatively large feedthrough voltage. The feedthrough voltage is

$$V_{FT} = \left(\frac{C_{gs}}{C_o}\right) V_{RST2} \qquad (4-1)$$

giving approximately V_{FT} = 0.7 volt for the two-element CCIRID (C_o = 10 pf) and 1.2 volt for the 20-element device (C_o = 6 pf). The feedthrough magnitude did not present a problem in the measurements since it was within the dynamic range of the electronics. It is generally desirable, however, to keep V_{FT} as small as possible and this is accomplished by keeping C_{gs} low. This may be achieved by incorporating a screen gate in the reset transistor and/or by keeping the gate-source overlap area small such as by self-aligned geometry.

The other waveforms in Figure 4-2 relate to operation either with detectors or electrical input and will be discussed in conjunction with the test results.

GATE OXIDE WITNESS EVALUATION

Twenty-element CCIRIDs from two lots were tested during this contract, 8585 Lot 8B and 8585 Lot 11B. Almost all data obtained as of this writing are for devices from Lot 8B, and both of the 20-element arrays delivered under this contract came from this lot; consequently, it is the better characterized of the two lots. The gate oxide witness samples for Lots 8B and 11B were 486B-25C and 532-2A, respectively, and data for both will be given. Witness sample gate oxide processing was identical to that of the CCIRID wafers as was discussed in Section 3.

8585 Lot 8B (Witness Sample 486B-25C)

To obtain a representative sample size, four dies from the Lot 8B witness sample 486B-25C were packaged in TO-5 headers for low-background C-V evaluation, identified as cans 1 though 4. At this point in the program,

there was concern about what effects the standard substrate contacting procedure had on the MOS characteristics, if any. Consequently, the standard procedure -- an indium solder contact, a known ohmic contact to n-type InSb but one requiring exposure to ~160°C -- was used on cans 1 and 2, and a conductive epoxy contact on cans 3 and 4.

The LTCVD SiO_2 gate oxide for 8585 Lot 8B (and 11B) was deposited in a horizontal-flow configuration reactor (AMS 2600), instead of the vertical-flow configuration AMS 1000 reactor used for the gate oxide deposition for 8585 Lot 4. These two reactors produce significantly different MOS charateristics on InSb, which is discussed further in Section 5. The horizontal-flow reactor results in a midband N_{ss} in the low 10^{11} cm^{-2}-eV^{-1} range as measured by the quasistatic method, compared to ~10^{12} cm^{-2}-eV^{-1} for the vertical-flow reactor. As will be shown later in this report, the measured low-frequency (or quasistatic) capacitance curves, from which N_{ss} is calculated, are influenced by the lateral inhomogeneity of the gate oxide and the N_{ss} values determined represent an upper bound to, but not the true, surface state density. As part of a 1978 Independent Research and Development project, detailed measurements of the surface state loss peaks by the conductance method showed that N_{ss} is in fact 10^{10} cm^{-2}-eV^{-1} or less for good samples produced with the horizontal-flow reactor.

In the horizontal-flow reactor, the reaction tends to be more homogeneous than that in the vertical-flow reactor*, which produces a less desirable SiO_2 deposit in terms of its mechanical and chemical properties: it is less dense and has a faster etch rate. Consequently, the two reactor types presented a tradeoff for CCIRID processing. Lots 8B and subsequent lots used the horizontal-flow reactor to gain the advantage of the lower surface state density, while the other properties of the oxide were known to be non-optimum.

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*This statement is true for the specific platen temperature (220°C) and gas flow rates used, and not for the two reactor types in general.

Figure 4-3 shows high-frequency (1 MHz) C-V curves for the seven 20-mil diameter capacitors in can 1 from sample 486B-25C. With the exception of dot 4, the flatband voltages are tightly grouped with $V_{FB} = -0.2 \pm 0.08$ volts. All capacitors were biased to -20 volts without breakdown (1.4×10^6 volts/cm).

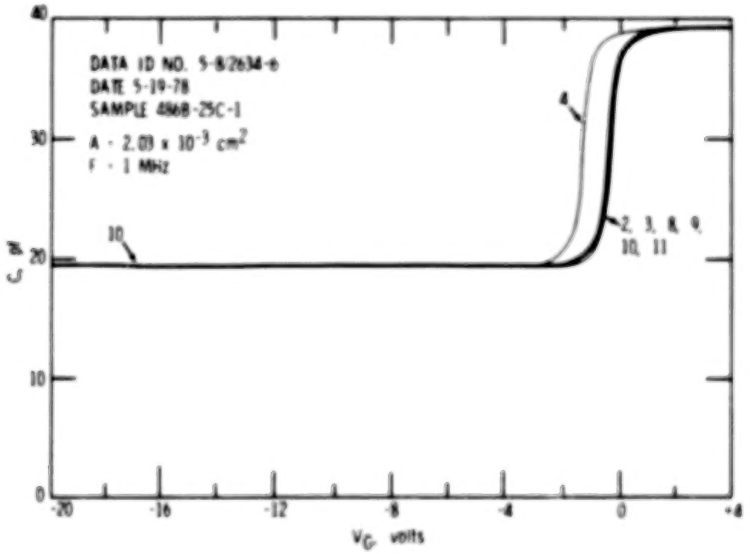

Figure 4-3. - High-Frequency C-V Curves for Gate Oxide Witness: 8585 Lot 8B; Sample 486B-25C (Can 1).

Figure 4-4 shows similar curves for can 2 of the same witness wafer, but on an expanded voltage scale and for all 11 pins of the TO-5 package. The nine-capacitor pattern consists of seven 20-mil diameter dots without guard rings (pin numbers 2, 3, 4, 8, 9, 10, and 11) and two smaller-diameter dots (pins 5 and 12) with guard rings (pins 1 and 6). The capacitor area listed in the figures (2.03×10^{-3} cm^2) applies to the seven unguarded dots. The mean flatband voltage of the eleven capacitors in can 2 is -0.055 volt with a standard deviation of 0.09 volt. For both can 1 and 2, the oxide capacitance is about 39 pf.

Figure 4-5 shows the measured low- and high-frequency C-V curves (dashed curves) for one capacitor in can 1, compared to the ideal (solid) low-frequency curve. Comparison with Figure 3-4 in the previous section

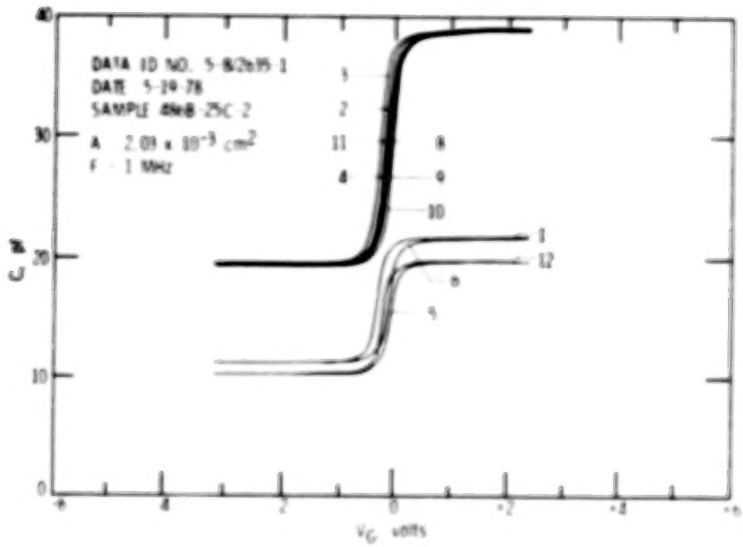

Figure 4-4. - High-Frequency C-V Curves for Gate Oxide Witness; 8585 Lot 8B; Sample 486B-25C (Can 2).

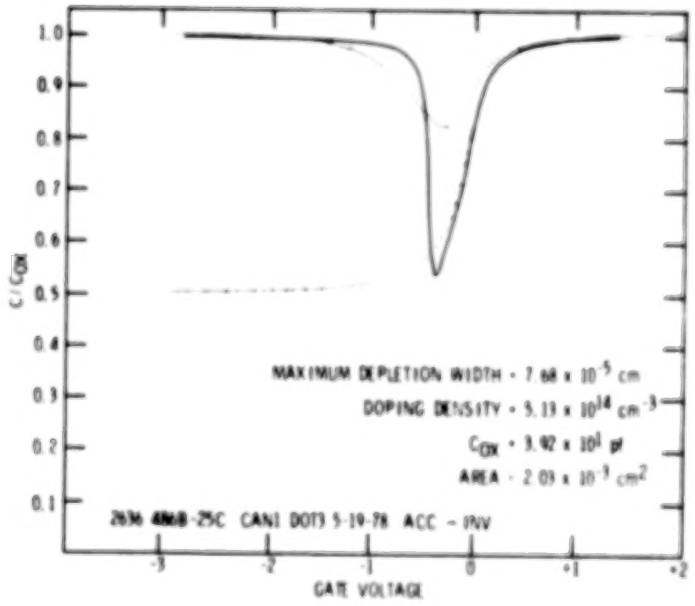

Figure 4-5. - Low-Frequency and High-Frequency C-V Curves for Gate Oxide Witness; 8585 Lot 8B; Sample 486B-25C (Can 1, Dot 3).

shows the improved characteristics of the horizontal-flow reactor gate oxide. The measured high-frequency characteristic in Figure 4-5 shows little dispersion from the ideal curve and, since the flatband voltage is very near zero, essentially overlies it, indicating a low surface state density. The measured low-frequency characteristic in Figure 4-5 shows a larger magnitude (and more symmetrical) dip compared to Figure 3-4, also consistent with lower N_{ss}, but the curve still departs significantly from the ideal ($N_{ss} = 0$) low-frequency curve. This departure is in fact due to the lateral nonuniformity of the horizontal-flow LTCVD SiO_2. Figure 4-6 shows the apparent surface state density calculated from the measured low-frequency curve of Figure 4-5, assuming that the low-frequency curve is solely being influenced by the surface-state capacitance C_{ss} (proportional to N_{ss}) and not by other non-ideal effects such as lateral inhomogeneity. Note that two curves are plotted, one labeled "LF" and the other "LF-HF." The "LF" curve is calculated by comparing the measured to the ideal low-frequency curve; the "LF-HF" is obtained by comparing the measured low-frequency and high-frequency curves.

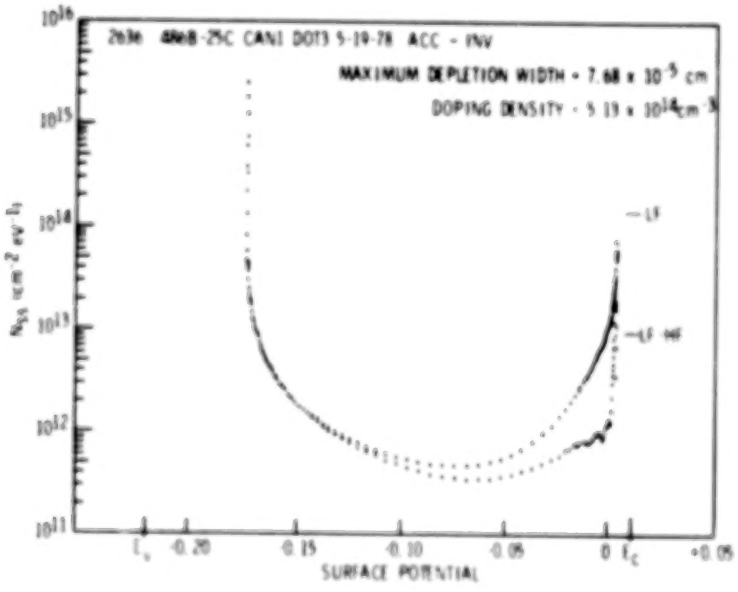

Figure 4-6. - Surface State Density by Quasistatic Technique of Gate Oxide Witness; 8585 Lot 8B; Sample 486B-25C (Can 1, Dot 31.

Good agreement between the two curves over most of the surface potential range serves to self-check the calculation. Midband N_{ss} from Figure 4-6 is 4×10^{11} cm^{-2}-eV^{-1} and, as stated, this represents an upper bound to the actual surface state density of 8585 Lot 8B. Figure 4-7 plots the quasistatic determination of N_{ss} for another capacitor in the same package, showing similar results.

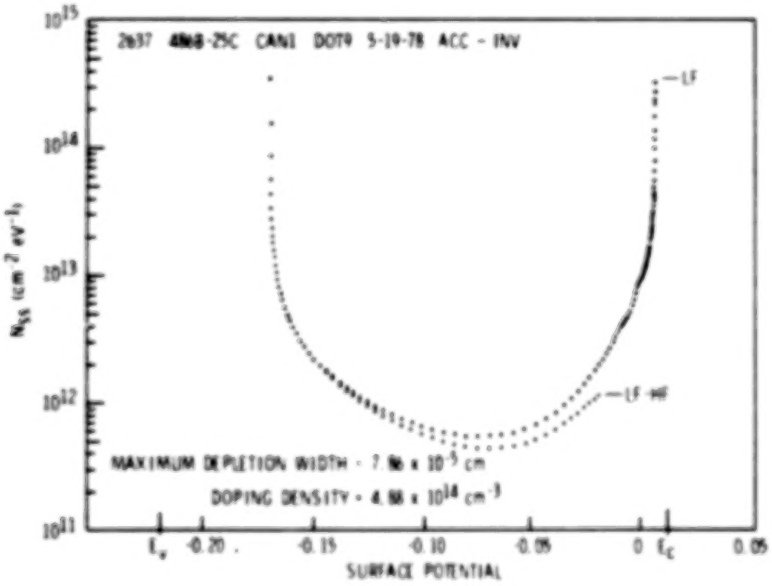

Figure 4-7. - Surface State Density by Quasistatic Technique of Gate Oxide Witness; 8585 Lot 8B; Sample 486B-25C (Can 1, Dot 9).

Figure 4-8 shows the C-V curves for the seven unguarded capacitors in 486B-25C can 4. The flatband voltage is zero and the uniformity is seen to be excellent. Note that the apparent oxide capacitance is lower (31 pf instead of the 39 pf for cans 1 and 2). This is an artifact associated with a high-resistance substrate contact, resulting from the conductive epoxy bond used for this can. The conductive epoxy contacts were found to be unreliable at cryogenic temperatures.

Finally, Figure 4-9 shows the hysteresis in the C-V characteristics for sample 486B-25C; all capacitors displayed identical hysteresis and the dot in

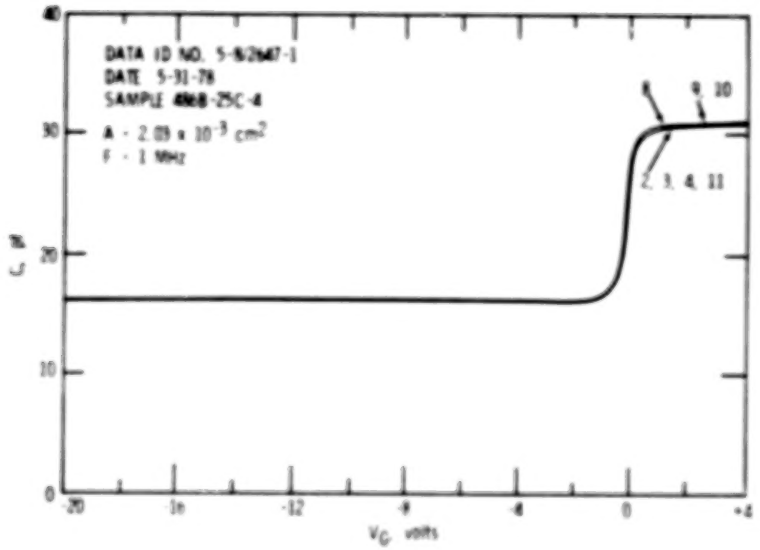

Figure 4-8. - High-Frequency C-V Curves for Gate Oxide Witness: 8585 Lot 8B; Sample 486B-25C (Can 4).

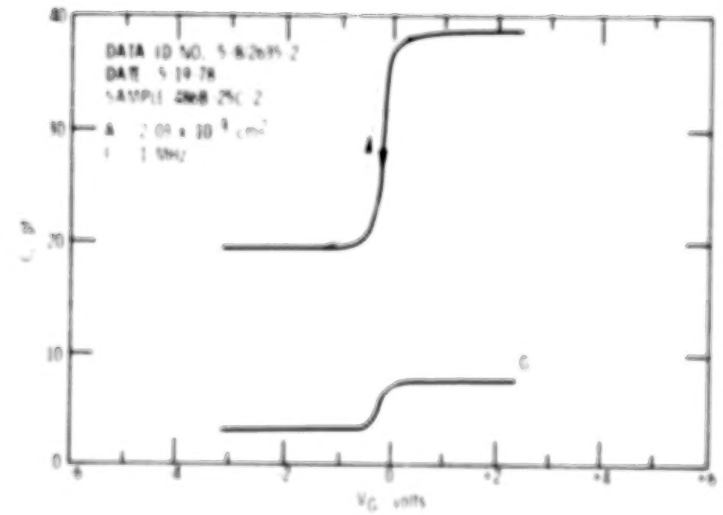

Figure 4-9. - Hysteresis of Gate Oxide Witness; 8585 Lot 8B; Sample 486B-25C (Can 2, Dot 11).

Figure 4-9 is representative. Gate oxides have been deposited in the horizontal-flow CVD reactor for which hysteresis is totally absent; however, sometimes relatively small hysteresis results as in the case of this particular deposition. The flatband shift in Figure 4-9 is $\Delta V_{FB} = 0.2$ volt. The solid curve is the positive-to-negative gate voltage sweep, and the dotted curve is the negative-to-positive return sweep.

8585 Lot 11B (Witness Sample 532-2A)

The characteristics of the witness sample for 8585 Lot 11B are shown in Figures 4-10 through 4-13. The flatband voltages ranged from zero to slightly positive (+ 0.3 volt). The dips in the measured low-frequency capacitance curves (Figure 4-10) are close in width to the ideal curve. An anomalous feature shown by this witness sample, however, is the presence of a secondary slope in the measured high-frequency curve extending from V_G 0 to -2 volts, in the weak inversion region. It is also reflected in the low-frequency curve (Figure 4-10). Figure 4-11 shows that the secondary slope in the high-frequency C-V curve corresponds to a localized band of apparent surface states centered about 0.05 eV above the valence band edge. Although the quasistatic calculation of surface state density becomes very inaccurate and should not in general be accorded any quantitative credibility near the band edges, there is a distinct plateau in the N_{ss} curve of Figure 4-11, where $N_{ss} \cong 5 \times 10^{12}$ from $\psi_s = -0.13$ to -0.17 volt, which is clearly absent in the previously discussed samples, Figure 3-5, 4-6, and 4-7. This is of unknown origin and occurred for several depositions for a time before and after the date of this sample (and lot) gate oxide deposition. Figure 4-12 shows the quasistatic surface state density for another dot from the same sample; the N_{ss} hump is likewise present (note the change in N_{ss} scale). Midband N_{ss} (again an apparent value) is 2.0- to 2.5 $\times 10^{11}$ cm^{-2}-eV^{-1}, lower than that of the witness sample for 8585 Lot 8B.

The anomalies in the curves of Figure 4-10 through 4-12 have not been observed recently. It should be pointed out that, in the earlier stages of the LTCVD SiO_2 process development, secondary humps and/or dips in the

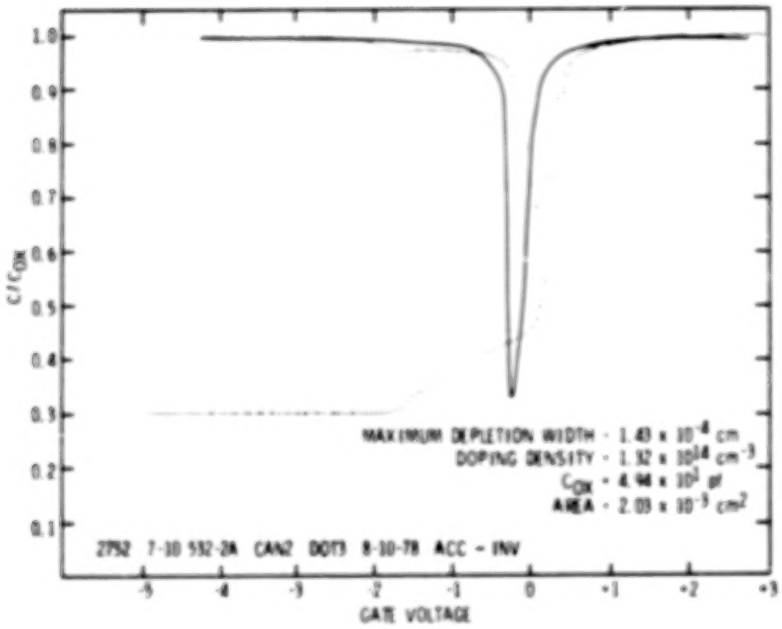

Figure 4-10. - Low-Frequency and High-Frequency C-V Curves for Gate Oxide Witness; 8585 Lot 11B; Sample 532-2A (Can 2, Dot 3).

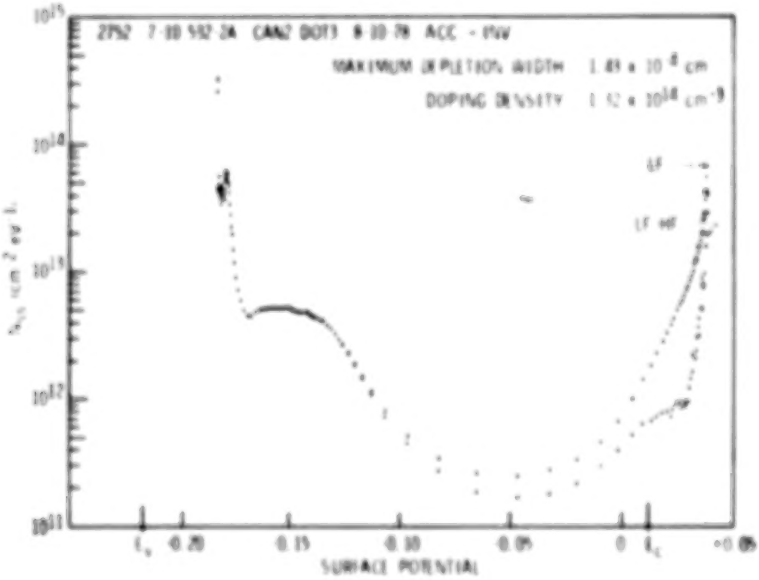

Figure 4-11. - Surface State Density by Quasistatic Technique of Gate Oxide Witness; 8585 Lot 11B; Sample 532-2A (Can 2, Dot 3).

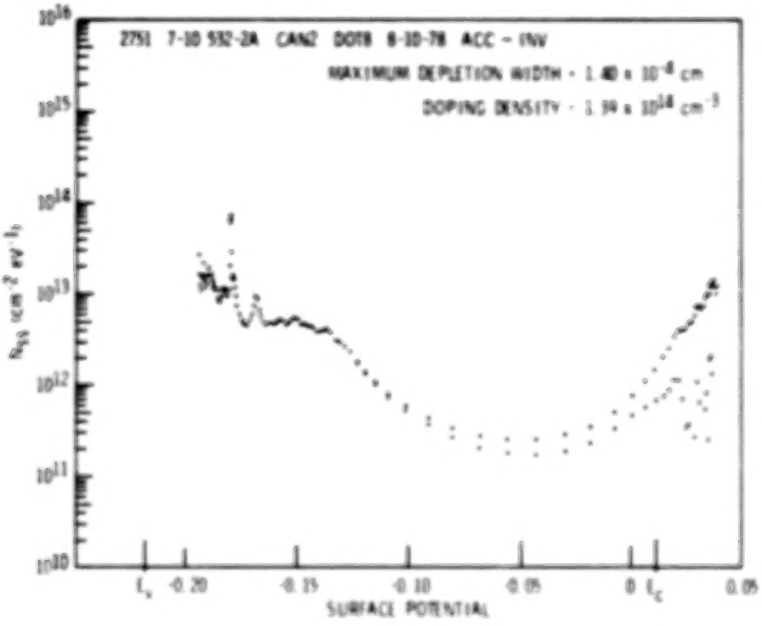
2751 7-10 532-2A CAN2 DOT8 8-10-78 ACC - INV
MAXIMUM DEPLETION WIDTH - 1.40 x 10^-4 cm
DOPING DENSITY - 1.39 x 10^14 cm^-3
SURFACE POTENTIAL

Figure 4-12. - Surface State Density by Quasistatic Technique of Gate Oxide Witness; 8585 Lot 11B; Sample 532-2A (Can 2, Dot 8).

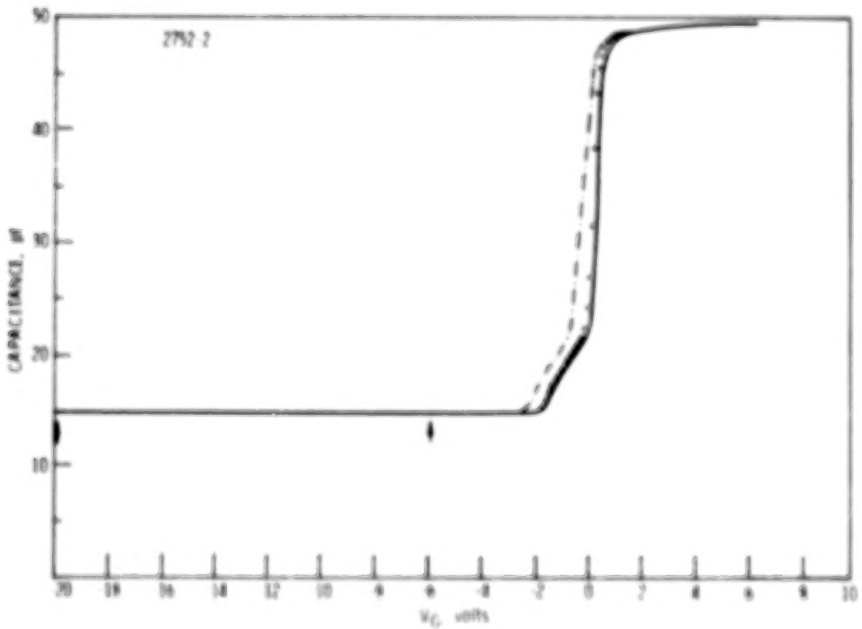

Figure 4-13. - Hysteresis of Gate Oxide Witness; 8585 Lot 11B; Sample 532-2A (Can 2, Dot 3).

low-frequency C-V characteristics and slope changes in the high-frequency curves were observed in vacuum baking studies to correlate with absorption of water. They could be reversibly removed and restored by vacuum baking at 100 °C and re-exposure to atmosphere, respectively. It is possible, therefore, that such contamination was present in Sample 532-2A (no vacuum baking studies were made).

The hysteresis of the witness sample No. 532-2A is shown in Figure 4-13, with the solid and dashed curves corresponding to the same sweep directions as in Figure 4-9. Two return (dashed) sweeps are shown, from V_G = -6 volts and -20 volts. The flatband voltage shifts are ΔV_{FB} = 0.2 volt and 0.5 volt for these two bias extremes.

GATE CAPACITANCE, FLATBAND VOLTAGE, AND SURFACE POTENTIAL DIAGRAM FOR 8585 LOT 8B

After completion of processing of 8585 Lot 8B, wafer probing, and dicing, three chips were mounted in TO-5 packages for evaluation of the channel stop metal, buried metal, and surface metal capacitors. These chips were from wafer 498-17, which also yielded several 20-element CCIRIDs. The oxide parameters for lot 8B, determined from these capacitors, are listed in Table 4-2.

The nominal oxide thicknesses (determined from sapphire witness substrates) are listed in row (a) of Table 4-2 and the measured gate capacitances in row (b). The capacitances per unit area of the channel stop, buried, and surface metal levels are seen to be very close to those of 8585 Lot 4 (compare to Table 3-11); however, the nominal oxide thicknesses associated with each level of Lot 8B are thinner than in the earlier lot, indicating that the dielectric constant is lower. This reduction is due to the less dense SiO_2 layer grown in the horizontal-flow configuration CVD reactor. Row (c) in Table 4-2 gives the dielectric constant associated with each gate level, calculated from the data in rows (a) and (b). It is seen to increase from 3.31 for the channel stop metal to 3.74 for the surface metal. The (average)

Table 4-2. Oxide Parameters, 8585 Lot 8B

	GATE OXIDE WITNESS	CHANNEL STOP METAL	BURIED METAL	SURFACE METAL
WAFER NO.	8868-25C	898-17	898-17	898-17
(a) NOMINAL OXIDE THICKNESS (Å)	1995	1995	2970	6420
(b) MEASURED C_{OX} (f/cm²)	1.98×10^{-8}	2.00×10^{-8}	1.31×10^{-8}	7.50×10^{-9}
(c) DIELECTRIC CONSTANT	3.86	3.91	3.51	3.78
(d) FLATBAND CAPACITANCE (C_{FB}/C_{OX})	0.675	0.774	0.686	0.91
(e) MEASURED V_{FB} (volts)*	-0.1	-1.9 -1.6	-1.8 -1.77	-0.96 -0.86
(f) N_{fc} (charges/cm²)*	$+1.2 \times 10^{10}$	$+1.7 \times 10^{11}$	$+1.1 \times 10^{11}$	$+2.6 \times 10^{10}$

*CALCULATED FROM (a) AND (b)

†UPPER NUMBER FOR POSITIVE TO NEGATIVE V_G SWEEP, LOWER NUMBER VICE VERSA

dielectric constant increases in this manner since the ratio of the sputtered SiO_2 thickness to the LTCVD SiO_2 thickness increases as the CCIRID structure is built up.

The measured flatband voltages are given in row (e) of Table 4-2. The flatband voltages are low as was the case for the earlier Lot 4. The associated fixed-charge densities (again assuming zero metal-semiconductor work function difference) are listed in row (f). Whereas N_{fc} was relatively uniform for Lot 4 and its witness sample ($N_{fc} \sim +1.1$ to $1.9 \times 10^{11}/cm^2$), for Lot 8B two of the gate levels (channel stop and buried metal) have a similar $N_{fc} \sim 10^{11}/cm^2$ while the witness sample and surface metal show N_{fc} in the low $10^{10}/cm^2$ range. This variation is undoubtedly due to upper-level processing variables but at this time we have insufficient statistics to correlate the effects of upper-level process steps on N_{fc}. The result, as relates to the operating voltages for Lot 8B, is that the flatband voltage of the surface metal is lower than that of the buried metal, opposite to the situation that would be normally obtained with a uniform N_{fc} for all gate levels.

In row (e) of Table 4-2, two V_{FB} values are listed for the three CCD gate levels corresponding to negative-going and positive-going gate voltage sweeps, reflecting the gate oxide hysteresis. Figure 4-14 shows the measured C-V curves for the three gate levels on one test capacitor chip (Chip C5). Figure 4-15 reproduces the computer plot of the measured low- and high-frequency, compared to the ideal, C-V curves for the surface metal capacitor on test chip C6. Figure 4-16 is the apparent surface state density calculated from Figure 4-15. Midband N_{ss} is 4×10^{11} cm^{-2}-eV^{-1} which is identical to the Lot 8B witness sample, Figures 4-6 and 4-7.

The fact that the apparent surface state density and hysteresis of the witness capacitors and the test capacitors on the completed CCIRID wafers are essentially identical allows the conclusion that the upper level fabrication process is to first order not affecting the InSb MOS characteristics. Some flatband voltage shifting is evident, which is not surprising considering that numerous dc and rf sputtering and rf plasma etching operations are involved in the upper level processing. For all lots to date, no annealing operations

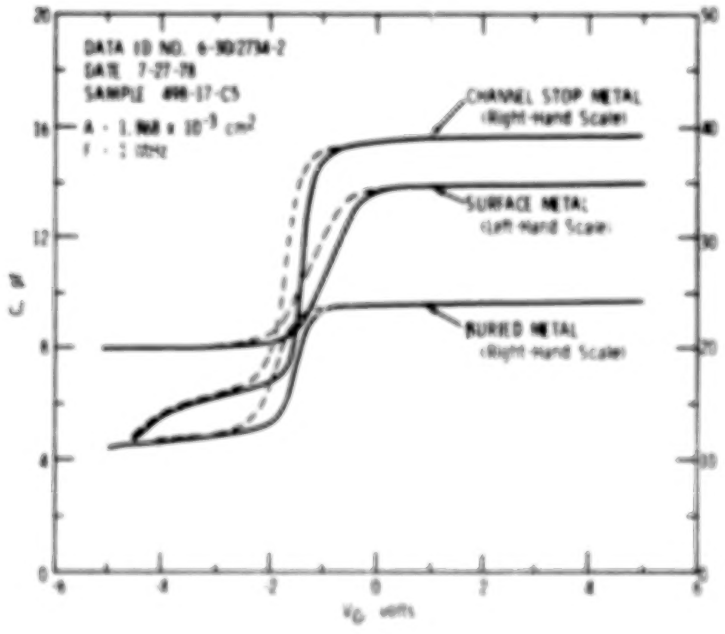

Figure 4-14. - C-V Characteristics of Channel Stop, Buried, and Surface Metal Capacitors; Wafer 498-17; 8585 Lot 8B; Chip C5.

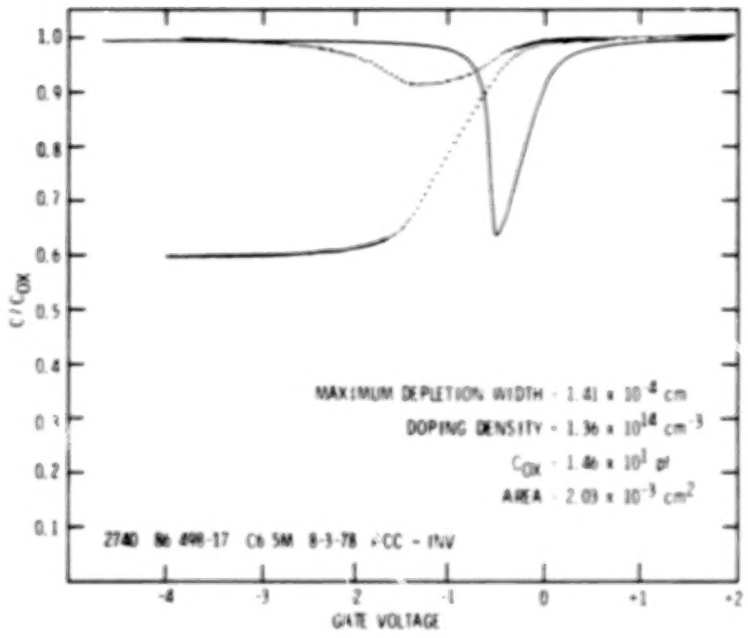
C/C_OX
GATE VOLTAGE
MAXIMUM DEPLETION WIDTH = 1.41 x 10^-4 cm
DOPING DENSITY = 1.36 x 10^14 cm^-3
C_OX = 1.46 x 10^1 pf
AREA = 2.09 x 10^-3 cm^2
2740 No 498-17 Cb 5M 8-3-78 ACC - INV

Figure 4-15. - Low-Frequency and High-Frequency C-V Curves for Surface Metal Capacitor; Wafer 498-17; 8585 Lot 8B; Chip C6.

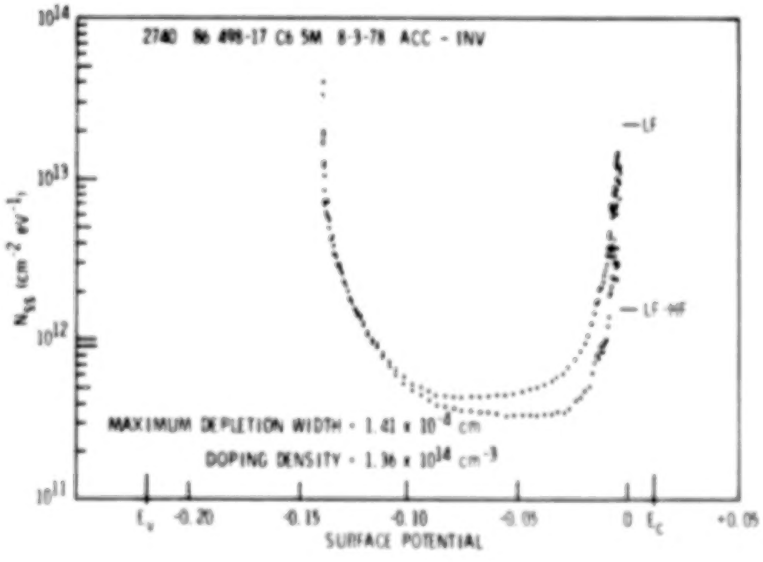
2740 No 498-17 Cb 5M 8-3-78 ACC - INV
LF
LF-HF
MAXIMUM DEPLETION WIDTH = 1.41 x 10^-4 cm
DOPING DENSITY = 1.36 x 10^14 cm^-3
SURFACE POTENTIAL

Figure 4-16. - Surface State Density by Quasistatic Technique of Surface Metal Capacitor; Wafer 498-17; 8585 Lot 8B; Chip C6.

were performed either during or after completion of the upper level processing. Future studies to correlate C-V characteristics with each upper level process step are required, along with investigation of intermediate or post-anneal steps to more accurately control flatband voltages of each gate level in the completed CCRIDs.

Using the parameters in Table 4-2 and equations (3-4) through (3-6), the surface potential plot for 8585 Lot 8B was calculated and is given in Figure 4-17. The substrate impurity concentration, C_{OXBM}, and C_{OXSM} are very nearly the same for lots 4 and 8B, and the slopes of the ϕ_s versus V_G curves in Figures 4-17 and 3-7 are similar. However, since the surface metal flatband voltage in Lot 8B is small, the ϕ_{SSE} curve in Figure 4-17 overlaps the ϕ_{SBE} curve. Because the device is 4¢ and does not require any built-in flatband voltage differences, device operation is not in any way affected by this.

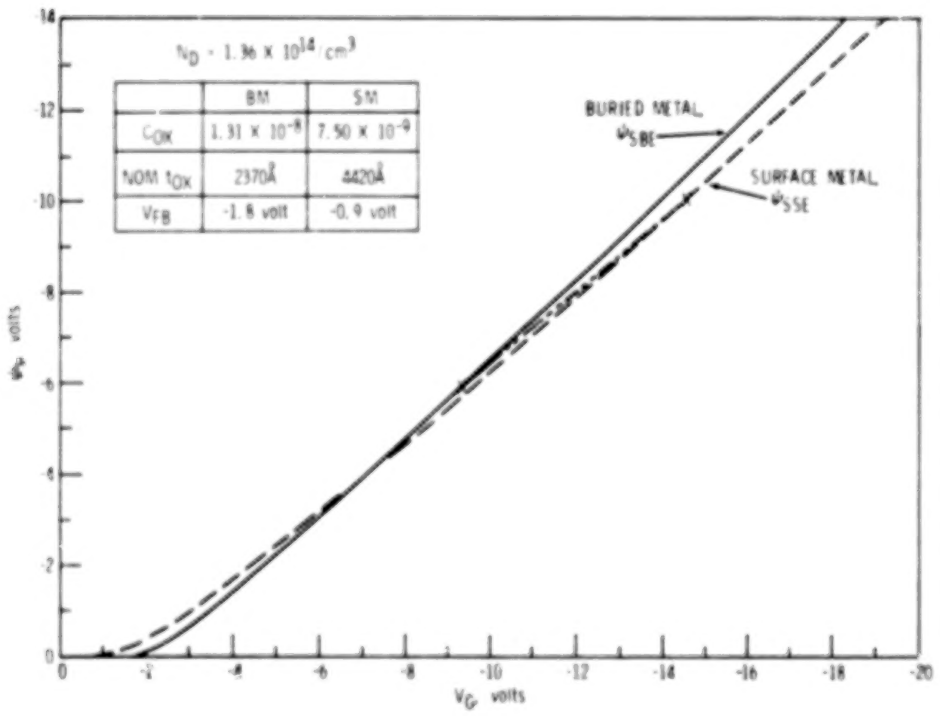

Figure 4-17.- Surface Potential versus Gate Voltage for Wafer 498-17, 8585 Lot 8B.

TEST EQUIPMENT CONFIGURATION

General Configuration

The general configuration that was used for testing the 20-element InSb CCIRIDs is shown in the block diagram of Figure 4-18. The array was tested in a specially-designed cryogenic dewar based on a Heli-Tran liquid helium transfer system*. The dewar, block A in Figure 4-18, contains: a cold stage with socket to accept CCIRID flatpack; low-temperature cavity surrounding the device; cold spectral bandpass filter; FOV restriction; intermediate temperature shield; and an intermediate temperature stage. A buffer/driver circuit is mounted on the intermediate temperature stage.

Clock waveforms and dc voltages necessary to drive the CCIRID, block B in Figure 4-18, were provided by commercially-available pulse generators and adjustable dc supplies. Two test sets were used during the course of the program, denoted as Test Sets 1 and 2. Test Set No. 1 is a rack-mounted set of pulse generators and dc supplies which provides all needed waveforms to operate the device. The rack includes a custom-built timing generator which provides properly-timed pulses for triggering the waveform generators. Set 1 does not contain any additional electronics for sampling or further processing of the CCIRID output waveform. When operating with Set 1, the device output waveform at point C in Figure 4-18 was displayed on an oscilloscope, or alternatively, at point D at the output of an offsettable voltage amplifier. Test Set 1 also includes a blackbody source and variable-speed chopper for optical evaluation of the CCIRIDs. This test set was used for most of the device testing in the program: for clock voltage/waveform optimization; for CTE measurement; and for optical mode evaluation. Set 1 does not include sample-and-hold (S/H) and other electronics plus computer interface necessary for noise or detectivity (D*) measurements. This equipment, block E in Figure 4-18, is incorporated in SBRC's CCD Array Test Set No. 2,

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*Heli-Tran System, manufactured by Air Products and Chemicals, Inc., Allentown, PA.

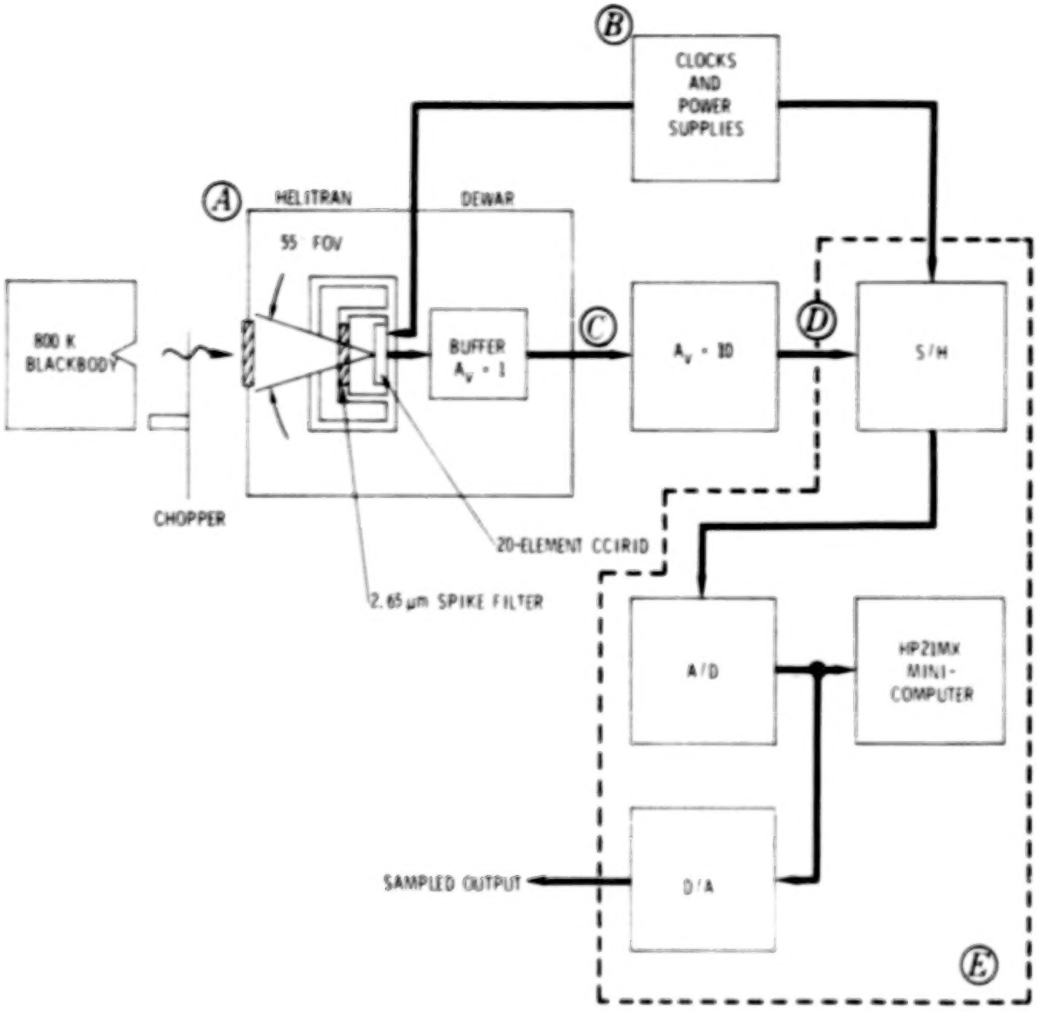

Figure 4-18.- General Test Configuration for 20-Element InSb CCIRID.

described later in this section, which also includes its own set of clocks and power supplies, block B.

The 20-element InSb CCIRID chips (with 3N163 MOSFETs) were mounted in 40-lead dual-inline flatpacks for testing in the Heli-Tran dewar. SBRC has standardized on the 40-lead DIPs for various CCD array programs where the lead count is sufficient to accommodate the input/output requirements. The particular flatpacks used were purchased from the 3M Company, Electronic Products Division, St. Paul, Minnesota, Part No. SZ-80220-AC, Multilayer Ceramic Dual-Inline Package, 40-lead, bottom-brazed.

During testing at SBRC, to facilitate optical inspection and chip access, the flatpacks were not provided with a window over the package well. The delivered CCIRIDs were provided with a 0.010-inch thick sapphire window epoxy-sealed over the well of the package. Window sealing was carried out in a nitrogen dry box. A photograph of a 20-element array mounted in the 40-lead DIP, with the sapphire window sealed over the well, is shown in Figure 4-19. Figure 4-20 shows a closer view of the InSb chip and MOSFETs in the flatpack well, prior to bonding of the sapphire window.

CCD Array Test Set 2

The CCD Array Test Set No. 2 was used for D* measurements described later in this section. A photograph of this test station in its original configuration is shown in Figure 4-21. The test console contains: a blackbody source and chopper; clock waveform generators; dc power supplies; a time mark generator; signal monitoring equipment; and test electrical generators to operate and test a wide variety of CCD arrays in both linear and area configurations. The helium storage dewar, transfer line, and Heli-Tran dewar resting on the blackbody source can be seen in the right-hand side of Figure 4-21. At the left of the Figure 4-21 is an HP9825 minicomputer which has been replaced with an HP21 MXE Minicomputer system since the photograph was taken.

A block diagram of the complete test station is shown in Figure 4-22. It is composed of: the IR source; the minicomputer system and interface equipment; the test console shown in Figure 4-21; monitoring oscilloscope; Heli-Tran dewar; and Heli-Tran Cart equipment.

In the CCD Test Console, timing signals, including a master clock, are generated by a switch-programmable timing generator, which supplies control signals to the: clock sources; CRT display; sample-and-hold; and analog-to-digital converter. Clocking pulses for driving the CCD are formed by nine Tektronix PG508 pulse generators capable of 50-MHz operation. Rise and fall times are adjustable as well as upper and lower pulse levels up to ± 20 volts. DC bias voltages are generated by twelve HP6215A adjustable

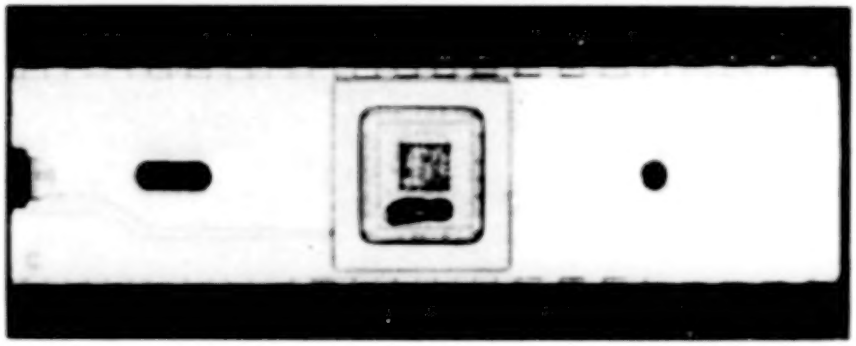

Figure 4-19.- 20-Element InSb CCIRID in 40-Lead Dual-Inline Package, with Sapphire Window Sealed Over Well.

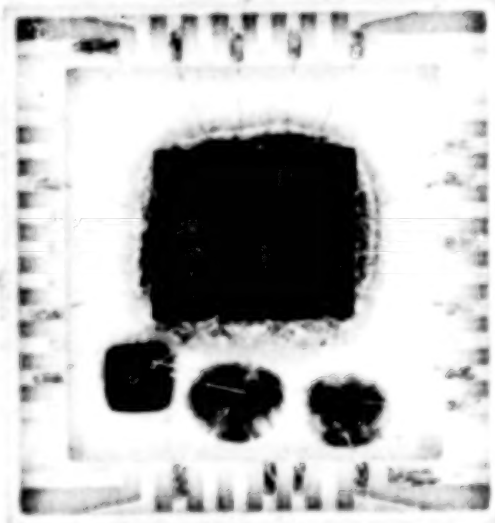

Figure 4-20.- 20-Element InSb CCIRID Mounted in Dual-Inline Package, Prior to Sealing of Sapphire Window.

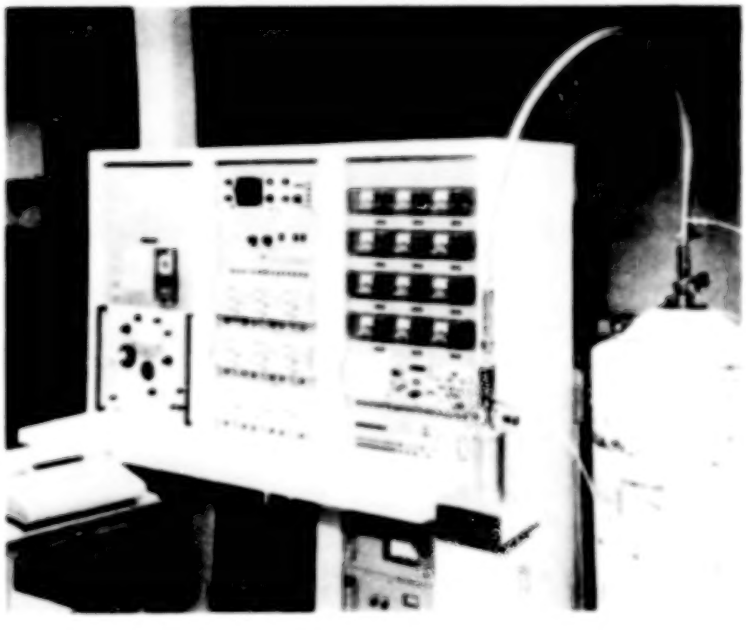

Figure 4-21.- CCD Array Test Set No. 2.

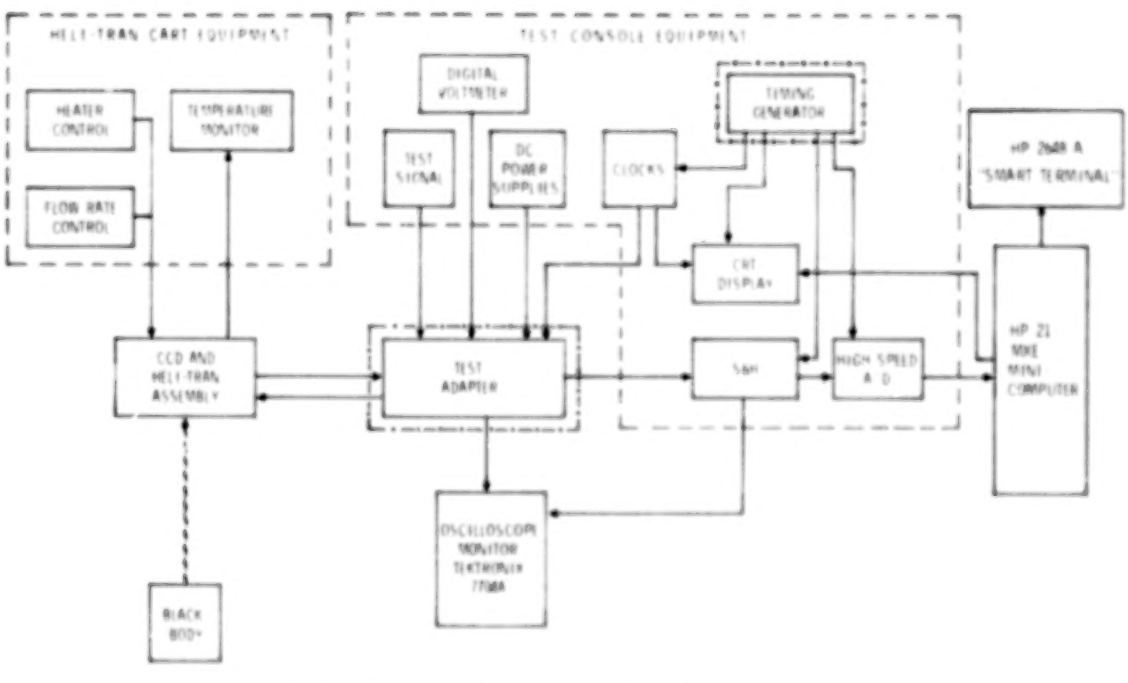

Figure 4-22.- Block Diagram of CCD Array Test Set No. 2 and Heli-Tran Cart Equipment.

regulated supplies. These are referenced inside the test adapter for each test configuration. A high-speed sample-and-hold/analog-to-digital converter is provided to digitize the CCD output to 13-bit resolution. Conversion time for each sample is less than 1 usec so that sample-and-hold feedthrough of the signal pulse will not occur during digitization. Digitizer outputs are connected to the computer via an optically isolated data bus. A thumbwheel channel selector is provided on the sample-and-hold panel to route the output of any single-array element to a panel jack for signal, noise, or spectrum analysis. The high-speed A/D converter, which has a 900-nsec conversion time, allows continuous and complete digital conversion at approximately a 1-MHz word rate.

The highlights of the HP MXE minicomputer are:

1. High-speed 192-k byte core memory
2. Dual 15-M byte storage discs
3. "Smart" Terminal. The terminal, HP2648A, contains preprogrammed statistics packages as well as intermediate storage data.

Heli-Tran Dewar

The Heli-Tran dewar was developed for rapid device cooldown and warm-up, and variable temperature control. The system consists of the following:

1. Helium storage dewar
2. Coaxial transfer tube
3. Cooling head
4. Active temperature controller
5. Digital cold stage readout

Liquid helium[*] is extracted from the storage dewar via the coaxial transport tube and flows through the heat exchanger in the cooling head. A portion of the boiloff is used to cool the outer section of the transport tube; the rest is

[*]Other cryogens can also be used resulting in different temperature ranges of operation.

exhausted. Inside the cooling head, shown in Figure 4-23, a control thermocouple and heater assembly are part of the active temperature control loop, and an additional thermocouple is provided for digital temperature readout.

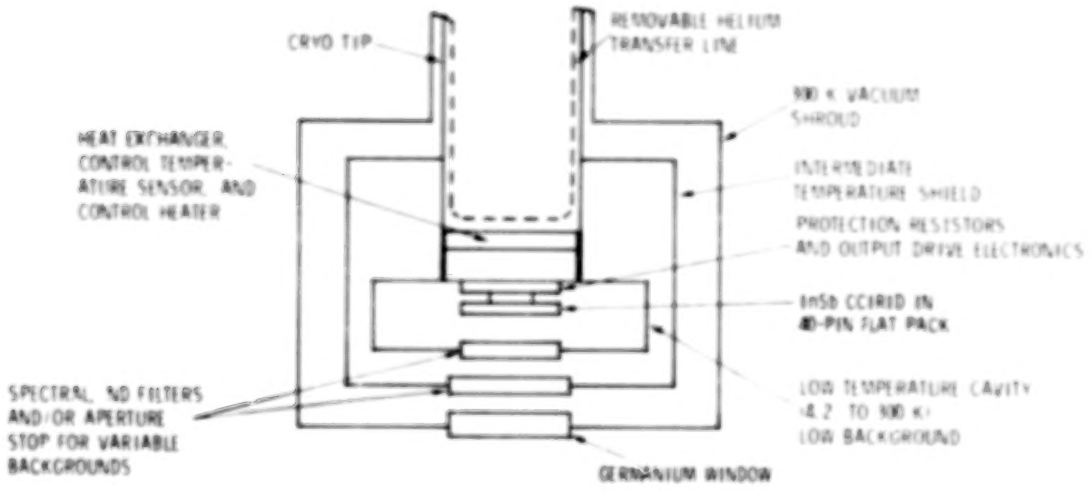
CRYO TIP
REMOVABLE HELIUM TRANSFER LINE
300 K VACUUM SHROUD
HEAT EXCHANGER CONTROL TEMPERATURE SENSOR AND CONTROL HEATER
INTERMEDIATE TEMPERATURE SHIELD
PROTECTION RESISTORS AND OUTPUT DRIVE ELECTRONICS
InSb CCD/RD IN 40-PIN FLAT PACK
SPECTRAL, ND FILTERS AND/OR APERTURE STOP FOR VARIABLE BACKGROUNDS
LOW TEMPERATURE CAVITY (4.2 TO 300 K) LOW BACKGROUND
GERMANIUM WINDOW

Figure 4-23. - Sketch of Low-Temperature Cavity, Shields, and Windows in Heli-Tran System.

Manually-controlled warm-up heaters are provided for rapid heating. The remainder of the cooling head is similar to a small dewar with a cold stage, on which the test device is located, separated by an intermediate stage. The cold stage accommodates the 40-pin dual in-line package and includes terminations and protective networks for each pin. The intermediate stage contains buffer/driver electronics and an interconnecting plated shield flat cable. The same type of cable is used to connect the test device to three 19-pin interface connectors.

Helium consumption after cooldown is approximately 1/2 liter per hour with normal heat loads. Typical cycle times (heat to 300 K, change sample, reevacuate and recool) are less than 1 hour.

Photon Flux Calculations

Optical evaluation of the 20-element CCIRIDs was carried out with low photon flux levels provided by a cooled 2.65-μm narrow bandpass filter mounted in the entrance window of the low-temperature cavity (Figures 4-18 and 4-23). This cavity and filter are thermally connected to the cold stage and reach array temperature. Sandwiched above the 2.65-μm narrow bandpass filter was a 1-inch diameter Pyrex glass plate which served to block any longer-wavelength passbands that the filter might have. The outer window of the dewar (Figure 4-23) was an 0.040-inch thick uncoated germanium plate.

The measured transmission $\tau(\lambda)$ of the combination of narrow bandpass filter, Pyrex plate, and germanium outer window is shown in Figure 4-24. Signal photon flux was provided by the blackbody set at 800 K. The total radiant emittance from a blackbody at this temperature is:

$$W_{bb} = \sigma T^4$$

$$= (5.6697 \times 10^{-12} \text{ watt cm}^{-2} \text{ K}^{-4}) T^4$$

$$= 2.322 \text{ watts/cm}^2 \text{ at } 800 \text{ K} \qquad (4\text{-}2)$$

or in terms of photons:

$$Q_{bb} = \sigma' T^3$$

$$= (1.52041 \times 10^{11} \text{ sec}^{-1} \text{ cm}^{-2} \text{ K}^{-3}) T^3$$

$$= 7.785 \times 10^{19} \text{ phot/sec-cm}^2 \text{ at } 800 \text{ K} \qquad (4\text{-}3)$$

The transmitted radiant emittance passed by the filter combination, W_{FILT} and Q_{FILT}, was calculated in the usual manner by integrating the 800 K spectral radiant emittance with the filter transmission curve of Figure 4-24:

$$W_{FILT}(800 \text{ K}) = \int W_\lambda (800 \text{ K}) \tau(\lambda) d\lambda$$

$$= 1.068 \times 10^{-2} \text{ watt/cm}^2 \qquad (4\text{-}4)$$

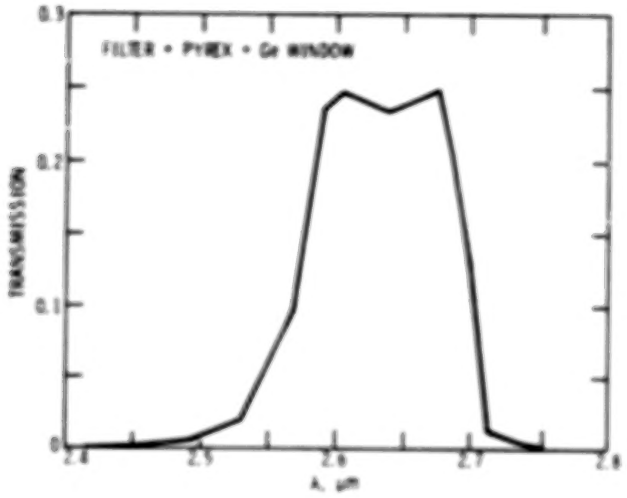

Figure 4-24. - Transmission Curve for 2.65-μm Narrow Bandpass Filter, Pyrex Plate, and Germanium Outer Window.

$$Q_{FILT}\,(800\ K) = \int Q_\lambda\,(800\ K)\,T(\lambda)\,d\lambda$$

$$= 1.416 \times 10^{17}\ \text{phot/sec-cm}^2 \qquad (4\text{-}5)$$

where $W_\lambda = \dfrac{C_1}{\lambda^5}\left(e^{C_2/\lambda T} - 1\right)^{-1}\ \text{wcm}^{-2}\mu\text{m}^{-1}$ (4-6)

$$Q_\lambda = \frac{C_1'}{\lambda^4}\left(e^{C_2/\lambda T} - 1\right)^{-1}\ \text{phot sec}^{-1}\text{cm}^{-2}\ \mu\text{m}^{-1} \qquad (4\text{-}7)$$

$C_1 = 3.7415 \times 10^4\ \text{wcm}^{-2}\mu\text{m}^4$

$C_2 = 1.43879 \times 10^4\ \mu\text{m K}$

$C_1' = 1.88365 \times 10^{23}\ \text{sec}^{-1}\text{cm}^{-2}\mu\text{m}^3$

and λ and T are in units of μm and K, respectively. Comparing (4-4) to (4-2) and (4-5) to (4-3) shows that the filter/window combination attenuates the blackbody radiant emittance by the factors $W_{bb}/W_{FILT} = 217$ and $Q_{bb}/Q_{FILT} = 550$.

The signal irradiance on the detector array depends on the blackbody aperture area (A_{aper}) and distance (D) from the aperture to the plane of the array:

$$H_{sig}, Q_{sig} = \frac{(W_{FILT}, Q_{FILT})A_{aper}}{\pi D^2} \qquad (4\text{-}8)$$

where either W_{FILT} or Q_{FILT} is used appropriate to whether energy or photon units are desired. For Test Set 1, D = 11.06 cm and the blackbody aperture diameters range from 0.380 to 0.0140 inch. Substituting in equation (4-8), Q_{sig} could therefore be varied from 2.70×10^{14} down to 3.66×10^{11} phot/sec-cm^2, or equivalenty H_{sig} from 2.03×10^{-5} to 2.76×10^{-8} watts/cm^2. For Test Set 2, D = 11.0 cm and apertures range from 0.200- to 0.0125-inch diameter resulting in a comparable range of signal flux levels. These are peak, rather than rms, signal flux levels. Figures and data in the following sections give the value(s) of Q_{sig} or H_{sig}, calculated using equation (4-8), corresponding to the blackbody aperture(s) used in the measurement.

The background photon flux incident on the array originates from the 300 K background viewed by the array through the 2.65-μm bandpass filter and field-of-view (FOV) restriction. The FOV in the dewar is established by the aperture in the intermediate temperature shield and is 55°. We first calculate Q_{FILT} (300 K) using the spectral radiant photon emittance of a 300 K-blackbody and $\tau'(\lambda)$ in the integral of equation (4-5). The transmission $\tau'(\lambda)$ is in this case higher by a factor of two compared to the signal flux calculation because the germanium outer dewar window is at ambient temperature and does not attenuate the background radiation. The result is:

$$Q_{FILT}\,(300\ K) = \int Q_\lambda\,(300\ K)\,\tau'(\lambda)d\lambda$$

$$3.3 \times 10^{12}\ \text{phot/sec-cm}^2 \qquad (4\text{-}9)$$

The background photon flux Q_B on the array is then calculated using

$$Q_B = Q_{FILT}\,(300\ K)\,\sin^2(\Omega/2) \qquad (4\text{-}10)$$

where Ω is the FOV. For $\Omega = 55^\circ$ the result is $Q_B = 7 \times 10^{11}$ phot/sec-cm^2.

Because of the possibility of radiation leaks, the background flux in the dewar was checked by mounting a photovoltaic InSb detector of known area and responsivity into a 40-lead flatpack and installing it in place of a CCIRID in the dewar. The calculated short-circuit current I_{sc} of the photodiode corresponding to $Q_B = 7 \times 10^{11}$ phot/sec cm^2 was 3 namp. After temperature stabilization of the low-temperature cavity and intermediate shield in the He i-Tran dewar, the measured I_{sc} of the test photodiode ranged from 2.0 to 5.1 namp, in reasonable agreement with the calculation, the latter current corresponding to 1.2×10^{12} phot/sec cm^2. Based on the calculations and measurements, the background for the measurements is nominally stated as 1×10^{12} phot/sec cm^2.

TEST RESULTS

Electrical Input

For clock optimization and determination of CTE, the shift registers of the 20-element CCIRIDs were first operated independently of the detectors by biasing off the transfer gate and photogate, and applying signal pulses to the fat zero input. The bottom waveform in Figure 4-2 shows the voltage applied to the input buried gate, illustrating the case of three charge packets being input. As with the two-element arrays, V_{ID} and V_{SC} were set to dc voltages for electrical input operation.

Figure 4-25 shows the output of device No. 498-17-A3 with ten voltage pulses applied to the FZ input. Twenty zeroes precede the first output pulse confirming proper operation of the shift register. This CCIRID was delivered to NASA in October 1978 as 20-element Serial No. 1. The output of Figure 4-25 is representative of device operation during the final testing, after

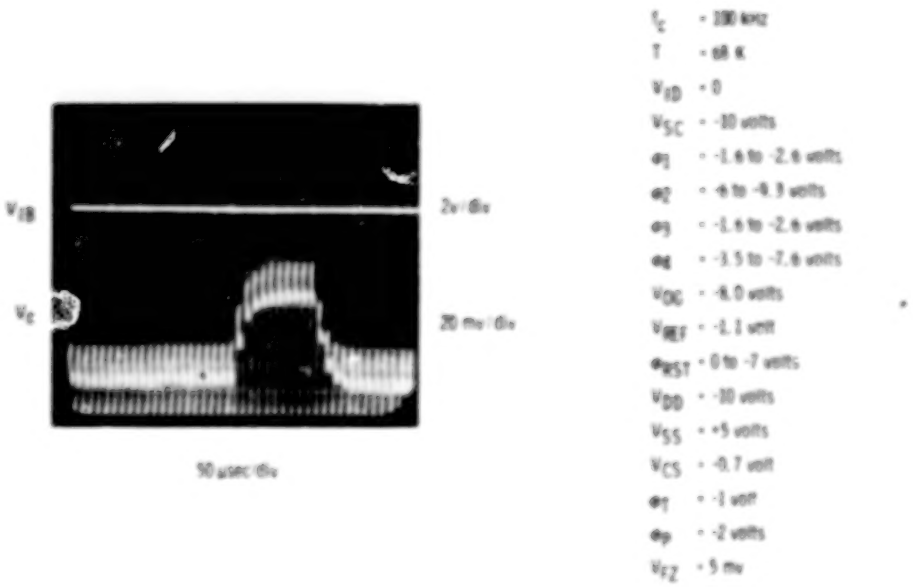

Figure 4-25. - Output of 20-Element InSb CCIRID No. 498-17-A3 with Ten Pulses Applied to FZ Input; CTE = 0.992 ± 0.002.

sealing the sapphire window to the flatpack. CTE as determined from both single and multiple charge packets introduced into the CCD was calculated to be 0.992 ± 0.002.

In February 1979 device 498-17-A3 was retested at SBRC with resulting outputs shown in Figure 4-26; the output for ten charge packets is reproduced in Figure 4-26(a) and that for a single charge packet in Figure 4-26(b). CTE was calculated to be 0.9955 ± 0.0005.

Testing of several other 20-element shift registers from wafer 498-17 indicated that device A3 is typical in terms of CTE. CTE for all the devices tested, and with various clock conditions, ranged from 0.990 to 0.996.

One 20-element array from the later lot 8585-11B, No. 522-20-B4, was bonded and similarly tested for CTE. Output waveforms for this device are shown in Figure 4-27. A comparable CTE was calculated from the output pulse trains for this CCD, CTE = 0.994 ± 0.001.

Good agreement was observed among the CTE values as calculated by the three methods discussed in Section 3; i.e., equations (3-12), (3-14), and

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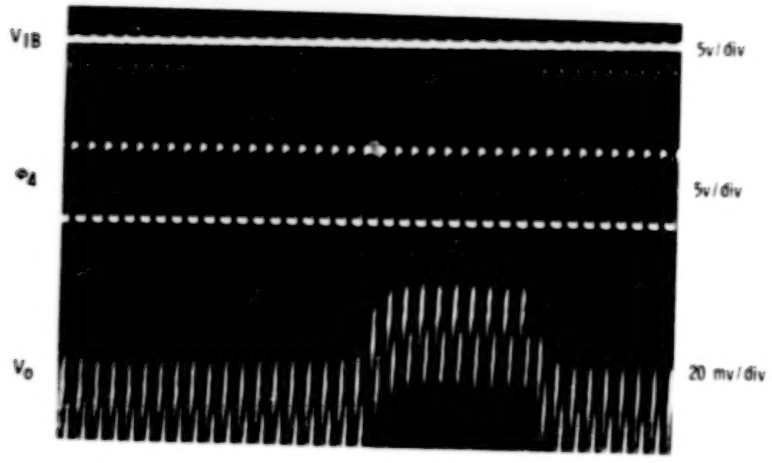
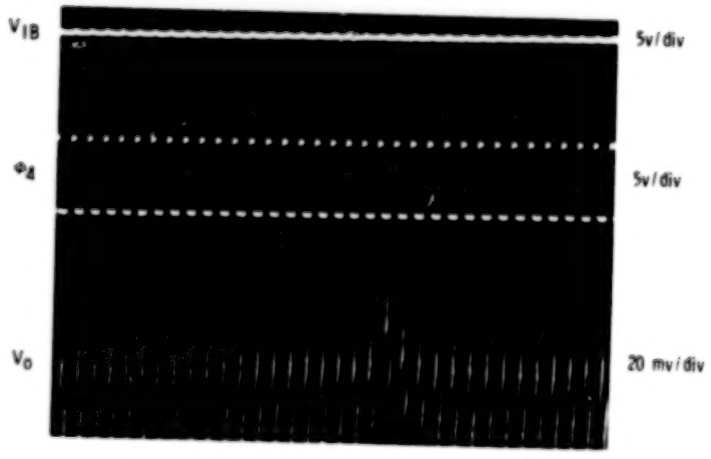


(a) TEN INPUT PULSES



(b) SINGLE INPUT PULSE

f_c	= 10 kHz	V_{OG}	= -4.4 volts
T	= 63 K	V_{REF}	= -1.0 volt
V_{ID}	= 0	Φ_{RST}	= -1.5 to -9.5 volts
V_{SC}	= -7.8 volts	V_{DD}	= -10 volts
Φ_1	= -0.8 to -2.6 volts	V_{SS}	= +5 volts
Φ_2	= -3 to -7 volts	V_{CS}	= -1.2 volt
Φ_3	= -0.6 to -2.0 volts	Φ_T	= 0
Φ_4	= -3 to -7 volts	Φ_P	= 0

Figure 4-26. - Output of 20-Element InSb CCIRID No. 498-17-A3 (Retest, Four Months after Packaging); CTE = 0.9955 ± 0.0005.

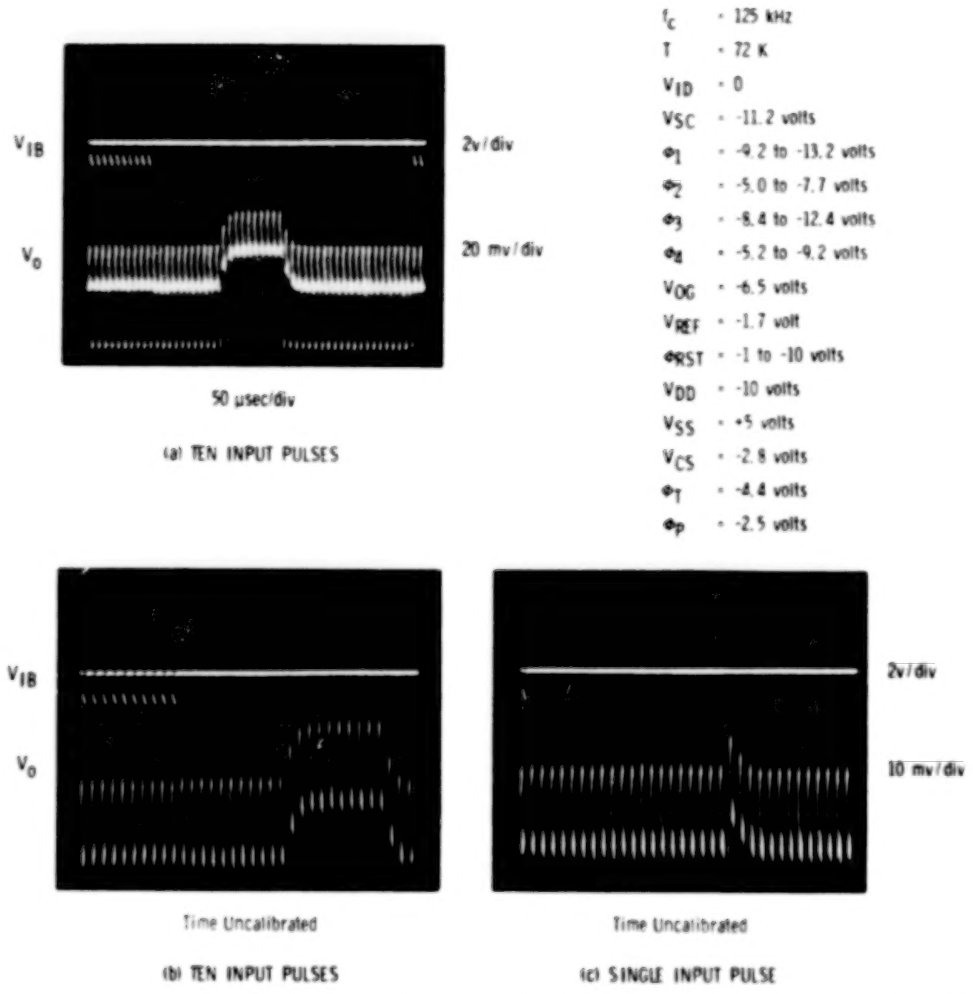


Figure 4-27. - Output of 20-Element InSb CCIRID No. 522-20-B4 with Signal Pulses Applied to FZ Input; CTE = 0.994 ± 0.001.

(3-16). The uncertainties listed along with each CTE value give the total range in the CTEs determined by the three methods, for the device operating under the given set of test conditions. CTE calculated by each method for the output waveforms in Figure 4-26 and 4-27 is listed in Table 4-3 as an example.

The absolute accuracy of the CTE values depends on the accuracy with which the pulse heights can be measured on the oscilloscope. Estimating the worst-case errors in determining the pulse heights, the resulting accuracy in determining the CTE varies by the method employed as follows:

Table 4-3. - Calculated Charge Transfer Efficiency

DEVICE NO.	FIGURE	EQUATION	CTE
498-17-A3	4-26 (a)	3-14	0.996
"	4-26 (a)	3-16, leaders	0.996
"	4-26 (a)	3-16, trailers	0.995
"	4-26 (b)	3-12	0.995
522-20-B4	4-27 (a)	3-14	0.994
"	4-27 (a)	3-16, leaders	0.994
"	4-27 (a)	3-16, trailers	0.993
"	4-27 (b)	3-14	0.994
"	4-27 (b)	3-16, leaders	0.994
"	4-27 (b)	3-16, trailers	0.995
"	4-27 (c)	3-12	0.995

Equation	Accuracy of CTE	(4-11)
3-12	±0.0007	
3-14	±0.0013	
3-16	±0.0007	

CCD Output Voltage and Charge Capacity

The output voltages observed for the 20-element CCIRIDs were approximately a factor of two higher than the levels for the two-element devices, in both the electrical and optical modes of operation. Assuming equivalent charge storage capacity per unit area for the two devices, a larger output voltage was expected for the 20-element array because 1) its CCD gate area is 30% larger than that of the two-element CCD, and 2) its output node capacitance C_o is smaller due to a change in wirebond arrangement in the flatpack.

Rather than using a spare lead of the Dual-Inline package as in intermediate tie point for the wirebonds between the output diode pad on the InSb chip and the two 3N163 MOSFETs, as was done for the two-element arrays, a small Ti-Au coated glass chip was mounted in the flatpack well to provide this tie point for the 20-element devices. This gold-coated chip is visible in the lower left-hand corner of the flatpack well in Figure 4-20. A wirebond first connects the output diode pad to the gold-coated chip; two additional wirebonds connect the gold-coated chip to the gate and drain pads of the source-

follower and switch transistors, respectively. The tie point was found to be necessary because the output diode pad on the InSb chip is not large enough to reliably accept two wirebonds. The capacitance of the gold-coated chip to ground is much smaller than that of a floating lead of the flatpack and its mating socket and provides a more favorable tie point.

The total CCD output capacitance (C_o) was calculated for the 20-element CCIRID using the known dimensions of the 8585 output diodes, gates, and pads and the characteristics of the 3N163 MOSFETs. The output capacitance is the sum of several terms:

$$C_o = C_{OD} + C_{PAD} + C_{SF} + C_{gs} + C_{CSM} + C_{stray} \qquad (4\text{-}12)$$

where C_{OD} = junction capacitance of output diode

C_{PAD} = capacitance of metal lead to output diode plus bonding pad

C_{SF} = source-follower input capacitance

C_{gs} = gate-to-source capacitance of switch transistor

C_{CSM} = output diode to channel stop metal capacitance

C_{stray} = stray capacitance

The p^+-n junctions in InSb produced by Be ion implantation have been shown by capacitance-voltage measurements to be abrupt, one-sided junctions obeying the familiar relationship:

$$C_{OD}/A_J = \left(\frac{q\epsilon_s N_D}{2(V_{BI} + V_R)}\right)^{\frac{1}{2}} \qquad (4\text{-}13)$$

For $\epsilon_s = 17.8\epsilon_o$, $N_D = 2 \times 10^{14}/cm^3$, $V_{BI} = 0.2$ volt and $V_R = 0$, equation (4-13) yields $C_{OD}/A_J = 1.123 \times 10^{-8}$ f/cm^2. The output diode is 1.9 × 2.0 mils or 2.45×10^{-5} cm^2 resulting in $C_{OD} = 0.28$ pf. Note that C_{OD} decreases as the square root of the reverse bias V_R, but C_{OD} does not decrease significantly from the $V_R = 0$ value for the reverse biases used.

The output diode bonding pad and metal lead interconnecting the junction contact with the pad comprises the largest capacitance contributing to C_o. This contribution will be essentially absent in subsequent InSb CCIRID designs

utilizing integrated output circuits. The pad and its metal lead are delineated on the buried metal level. (The overlying insulator is subsequently etched over the buried metal output diode pad and contacted by pad metal.) The bonding pad area is 5 × 5 mils or 1.61×10^{-4} cm^2, and the area of the metal line leading to the output diode is 7.2×10^{-5} cm^2 giving a total area of 2.33×10^{-4} cm^2. The cumulative oxide thickness under the buried metal pad and lead is (for 8585 Lot 8B) 3350Å (the oxide in this region is not etched as it is in the CCD channel), resulting in

$$C_{PAD} = \frac{K_{OX}\epsilon_o A_{PAD}}{t_{PAD}} = 2.24 \text{ pf} \qquad (4\text{-}14)$$

The dielectric constant K_{OX} in this calculation has been interpolated from the data in row (c) of Table 4-2.

The silicon 3N163 MOSFETs contribute the C_{SF} and C_{gs} capacitances. From the manufacturer's (Siliconix, Inc.) data sheets, the source-follower input capacitance C_{SF} was calculated to be 1.9 pf including the effect of Miller Feedback with $1\text{-}A_v \cong 0.1$. Also from the data sheet, $C_{gs} = 0.7$ pf.

The output diode to channel stop metal capacitance, C_{CSM}, arises from the necessary overlap of the p^+ region by the CSM, which is 0.2 mil on the 8585 layout. The effective perimeter is 6.8 mils giving an overlap area of 8.8×10^{-6} cm^2. From Table 4-2, the capactiance is 2.1×10^{-8} f/cm^2 resulting in $C_{CSM} = 0.2$ pf. The capacitance of the output diode to the buried metal output gate, resulting from a small overlap area, is much less than C_{CSM} and is neglected.

Stray capacitance, arising from the wirebonds and gold-coated chip (bond tie point) is estimated as ~1 pf based on previous experience. Summing the contributions to C_o gives 6.32 pf. We take 6 pf to therefore represent a reasonable estimate of C_o.

The gate area of the 20-element CCD is 0.5 × 4.2 mils or 1.35×10^{-5} cm^2 compared to 1.03×10^{-5} cm^2 for the two-element device.

Combined with the lower estimated capacitance, the output voltage levels of the 20-element array should be higher by the approximate factor (1.35/1.03) × (10/6) = 2.18 if the CCD charge capacity is the same. This is in good agreement with observed output voltages for the two devices. The maximum observed output voltage swing with electrical input was 60 mv for the 20-element CCIRIDs compared to 30 mv for the two-element device. Corresponding values for optical input were 50 mv and 25 mv, respectively. Using equation (3-17), a 60-mv output swing with C_o = 6 pf corresponds to a charge

$$\frac{Q}{q} = \frac{V_o C_o}{0.9q} = 2.5 \times 10^6 \text{ holes} \qquad (4\text{-}15)$$

Investigation of the correlation between charge capacity estimated from the surface potential diagram (Figure 4-17) and that calculated from the magnitude of output voltage [equation (4-15)] has not yet been carried out in detail over the range of clock conditions. A calculation was made under the one set of clock conditions for which V_o = 60 mv, device No. 498-17-A3, which indicated agreement to within 6%, confirming the general validity of the surface potential diagrams and the calculations leading to equation (4-15).

With regard to the interband tunnel current calculations of Section 2, study of the surface potentials corresponding to the clock voltages recorded throughout operation of the various devices (both two-element and 20-element) -- referring to the potential diagrams Figures 3-7 and 4-17 -- indicated that proper CCD operation was maintained with empty-well surface potentials under either buried or surface metal gates, or both, in the range of -6.0 to -8.3 volts, averaging -7.0 volts. Increasing a particular clock voltage an additional 1 or 2 volts beyond this point produced no change, but beyond this the dynamic range at the output was observed to decrease. Whether the additional charge for the high clock levels results from thermal mechanisms, tunneling, or avalanching remains to be ascertained from detailed studies in this bias regime. In the interim, apparent freedom from substantial interband tunneling out to ψ_s = -8 volts is consistent with the calculations leading

to Figure 2-3. Such a calculation must be considered as a first-order approximation to the actual situation in the device for at least three reasons:

1. Anderson's development considers fields only in the x-direction, i.e., such as for a capacitor or gate of infinite extent in the y- and z-directions. In an actual CCD, even with all other conditions being ideal, electric fields exist both in the y- and z-directions as well: tangential fields at the channel edges, and tangential fields established between gates during the transfer operation. Considerably more detailed calculations are required to include all the fields in a dynamic CCD model and to relate them to possible tunneling and/or avalanching mechanisms, but it is possible that these fields can be higher than that in the x-direction considered in Figure 2-3.

2. It is discussed in Section 5 that the MOS flatband voltages, up to this point in the report discussed as a precise value V_{FB}, are for the present devices characterized by a mean flatband voltage $\overline{V_{FB}}$ and a near-Gaussian distribution about the mean. This has several effects. In terms of the empty-well surface potentials associated with CCD operation, the effect translates to an average $\overline{\phi_{SSE}}$ and $\overline{\phi_{SBE}}$ with corresponding distributions about these mean surface potentials. If for example $\overline{\phi_{SBE}}$ = -8 volts, some regions beneath the buried gate may have local surface potentials of -9 volts or -7 volts; the former regions will have a higher tunnel current density than that associated with the average ϕ. This effect likewise complicates the first-order calculation in Section 2.

3. Material imperfections or inhomogeneities if present can create locally-higher electric fields with effect similar to (1) and (2).

Optical Input: Multiplexing Mode

The photogates and transfer gate of the 20-element CCIRID being independent of the CCD shift register allows the device to be operated in either a multiplexing or TDI mode, as was discussed in Section 3. Most device operational testing during this contract used the former clocking mode. The top two waveforms shown in Figure 4-2, the ϕ_P and ϕ_T clocks, are appropriate to the multiplexing mode where either $T_{INT} = N_B T_C = 20T_C$ for repetitive multiplexing (integration time equal to readout time) or $T_{INT} > 20T_C$ for integration times exceeding readout time.

Referring to Figure 4-2, the CCIRID photogate ϕ_P is clocked to voltage V_{P2} (approximately -5 volts for wafer 498-17) during the integration period to form the collecting deep depletion regions beneath the semitransparent

gates. At the end of an integration time, the accumulated signal charges in all twenty detectors are transferred simultaneously into the register by turning on the transfer gate in phase with CCD phase ϕ_4 (the detector input ports are under the ϕ_4 buried metal). The detector signal charges are then transferred out of the CCD at rate f_c. The first output signal is from the detector nearest the output (arbitrarily denoted detector No. 20) and, 20 clock periods later, the last output signal from detector No. 1. If $T_{INT} = N_B T_C$, successive samples from detector Nos. 20, 19, etc., will follow without intervening zeroes; when $T_{INT} > N_B T_C$, the output pulse train will be followed by a number of zeroes until the transfer gate initiates the transfer and readout cycle again. This latter is the case for the output pulse trains illustrated in this section. Trailers will be seen following the output pulse train established by the register's CTE. The output signal pulses originating from each detector in the array may then be sampled by a S/H circuit once each integration time or integral number of integration times; for example, detector No. 20 is shown being sampled and held in Figure 4-2.

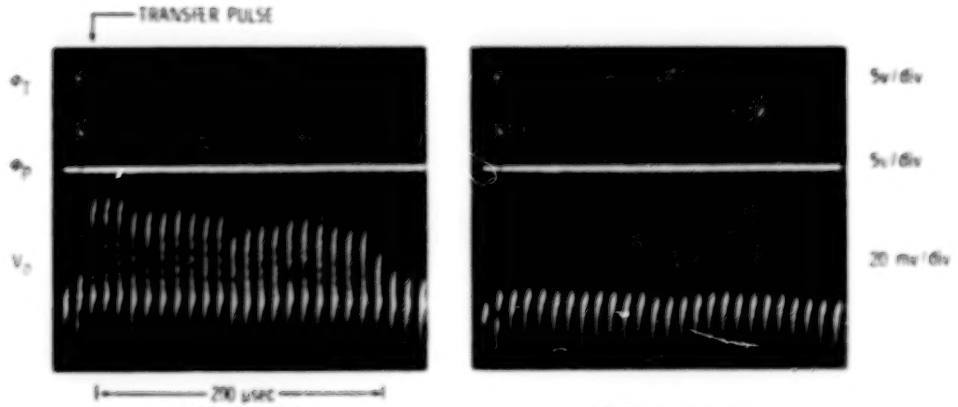
After establishing CCD clock levels ϕ_1 - ϕ_4 for optimum CTE using electrical input, for most devices tested only very small changes, if any, were needed in one or more clocks to optimize the output pulse train in the optical mode of operation. With ϕ_1 - ϕ_4 set at their levels determined from the electrical input test, and with no change in output circuit parameters (V_{OG}, ϕ_{RST}, V_{REF}), the test pulses were first removed from the input buried gate by setting $V_{IB2} = V_{IB1}$. Then ϕ_P was set at a dc level a few volts more negative than the buried metal flatband voltage, and ϕ_T was pulsed from $V_{T1} \cong$ surface metal flatband voltage to V_{T2}, 3 or 4 volts more negative than V_{T1}, as starting parameters. For a given signal photon flux level, integration time, and temperature, ϕ_P and ϕ_T were then adjusted for maximum signal magnitude and uniformity, while at the same time examining and minimizing dark current with the blackbody aperture covered.

Fat zero charge can be introduced into the register either optically or electrically. Background flux Q_B introduces an optical FZ charge which

increases linearly with Q_B and integration time. Because of the relatively low $Q_B = 10^{12}$ phot/sec cm^2 and the range of integration times explored in the present tests, the optical FZ was negligible and the FZ input was utilized. With $V_{ID} = 0$, the dc levels of V_{IB} and V_{SC} were adjusted to leak in the small (~10%) FZ level to minimize the output pulse train trailers.

A final remark with respect to the clock diagram of Figure 4-2 is that improved operation was obtained by clocking the photogate ϕ_P from V_{P2} to V_{P1} as shown although detector signals were observed with ϕ_P held at a dc voltage V_{P2}. ϕ_T is first switched from V_{T1} to V_{T2} followed by ϕ_P being dropped from V_{P2} to V_{P1}. This creates a push-clock, instead of a drop-clock, transfer mode where the charge is pushed out of the photogate, into and across the transfer gate, and thus into ϕ_4, when ϕ_P switches from V_{P2} to V_{P1}.

Operation of 20-element CCIRID No. 498-17-A3 in the multiplexing mode is shown in Figures 4-28 through 4-30 for three different temperatures, integration times, and CCD clock frequencies. In each figure, the oscilloscope photograph on the left is with the array illuminated by the blackbody (Q_{sig} is listed in each figure), and on the right, with the blackbody aperture blocked. In Figure 4-28, the IR signal was chopped with the chopper running at a low frequency $f_{chop} \ll T_{INT}^{-1}$; in the other two figures the chopper was not running, giving a dc signal flux. The top two waveforms in each photograph are the transfer gate and photogate clocks. In each case $T_{INT} > N_B T_C$, varying from 50 to 70 T_C. In the figures, readout of all 20 detectors is evident. The magnitude of the trailers correlates with the CTE measured by means of the electrical input. Although the array characteristics versus temperature have not been systematically studied up to this point (T_{INT}, f_c, Q_B, and T are all interdependent variables and a considerable characterization effort will be necessary to establish performance versus temperature), devices have been operated from the nominal temperature of 77 K to <10 K. At 77 K, dark current is seen in the output (Figure 4-30), and presently-available devices show better performance at temperatures in the range of

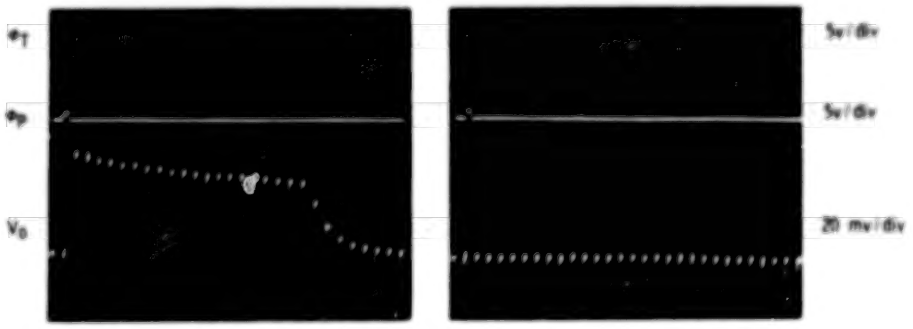


T_{INT} = 700 μsec = 70 T_C

Q_{sig} = 2.7 x 10^{14} ph/sec cm^2

f_c	= 100 kHz	Φ_3	= -2.4 to -4.4 volts
T	= 60 K	Φ_R	= 4 to -9.2 volts
V_{ID}	= 0	V_{OG}	= 6.2 volts
V_{IB}	= -3.7 volts	V_{REF}	= 1.6 volt
V_{SC}	= -2.9 volts	Φ_{RST}	= -1 to -10 volts
Φ_1	= -2.4 to -4.4 volts	V_{DD}	= -10 volt
Φ_2	= -4 to -9.2 volts	V_{SS}	= +5 volts
		V_{CS}	= -1.6 volt

Figure 4-28. - 20-Element CCIRID No. 498-17-A3 Operating at 60 K in Multiplexing Mode with Chopped IR Signal Input.



T_{INT} = 5 ms = 50 T_C

Q_{sig} = 3.7 x 10^{13} ph/sec cm^2

f_c	= 10 kHz	Φ_R	= -4 to -9.2 volts
T	= 40 K	V_{OG}	= -6.2 volts
V_{ID}	= 0	V_{REF}	= -1.6 volt
V_{IB}	= -3.7 volts	Φ_{RST}	= -1 to -10 volts
V_{SC}	= -2.9 volts	V_{DD}	= -10 volts
Φ_1	= -2.4 to -4.4 volts	V_{SS}	= +5 volts
Φ_2	= -4 to -9.2 volts	V_{CS}	= -1.6 volt
Φ_3	= -2.4 to -4.4 volts		

Figure 4-29. - 20-Element CCIRID No. 498-17-A3 Operating at 40 K in Multiplexing Mode, $T_{INT} > N_B T_C$.

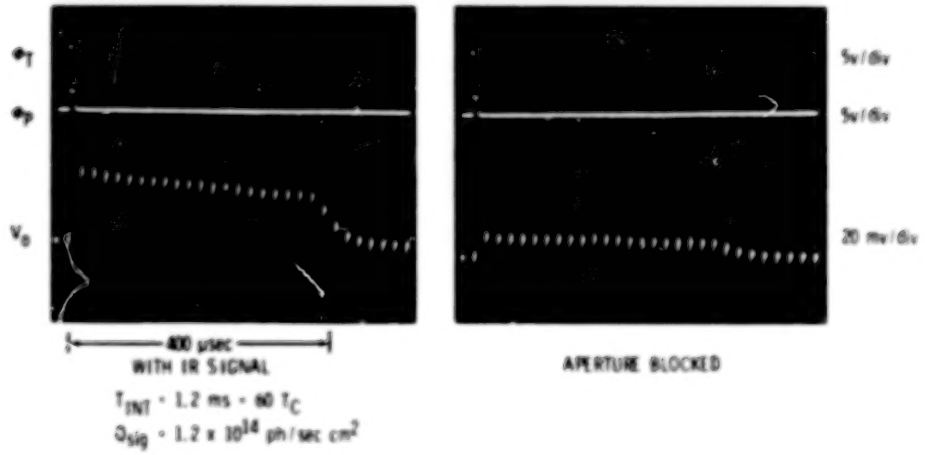


Figure 4-30. – 20-Element CCIRID No. 498-17-A3 Operating at 77 K in Multiplexin; Mode, $T_{INT} > N_B T_C$.

60 to 72 K, where most of the measurements have been made to date. The lower-than-nominal operating temperatures are due to the typical device storage times (a measure of dark current) on the wafers processed in this contract being considerably shorter than the values predicted from material parameters, as well as storage times measured on selected high-quality InSb substrates. This situation has been correlated with substrate properties and is discussed further in Section 5.

The output characteristic of another 20-element CCIRID from 8585 Lot 8B, 498-17-B2, is shown in Figure 4-31, with all test conditions listed in the figure. In this case, the temperature has been reduced and the clock frequency decreased to ~1 kHz, allowing a relatively long integration time

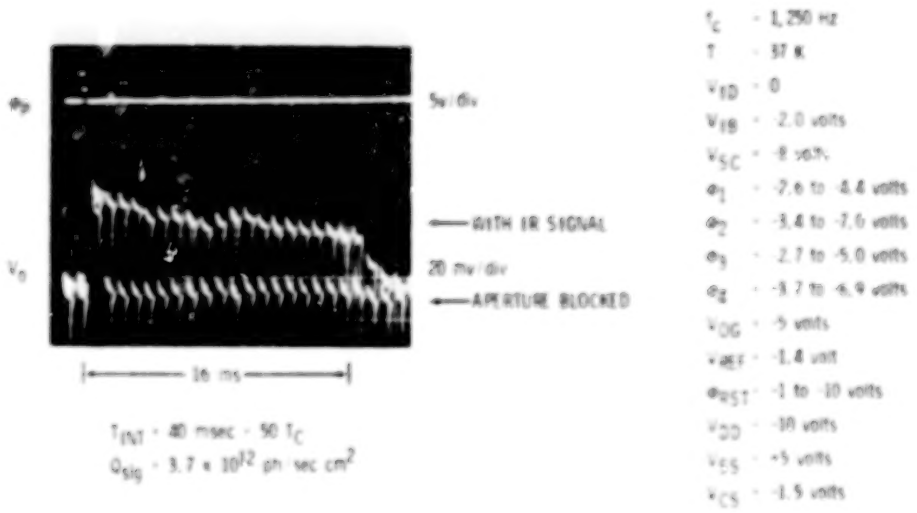

Φ_p
V_o
5v/div
WITH IR SIGNAL
20 mv/div
APERTURE BLOCKED
16 ms
T_{INT} = 40 msec = 50 T_C
Q_{sig} = 3.7 x 10^{12} ph/sec cm^2
f_C = 1,250 Hz
T = 37 K
V_{ID} = 0
V_{IB} = 2.0 volts
V_{SC} = 8 volts
Φ_1 = -7.6 to -8.4 volts
Φ_2 = -3.4 to -7.6 volts
Φ_3 = -2.7 to -5.0 volts
Φ_R = -3.7 to -6.9 volts
V_{OG} = -5 volts
V_{REF} = -1.4 volt
Φ_{RST} = -1 to -10 volts
V_{DD} = -10 volts
V_{SS} = +5 volts
V_{CS} = -1.5 volts

Figure 4-31.- 20-Element CCIRID No. 498-17-B2 Operating at 37 K in Multiplexing Mode, $T_{INT} > N_B T_C$.

T_{INT} = 50 T_C = 40 msec*. This illustrates the very high responsivities that can be obtained with integrating arrays such as the InSb CCIRID. The generally used figure-of-merit describing the responsivity of IR detectors is the voltage responsivity

$$R_\lambda = \frac{V_s}{H_{sig} A_D} \tag{4-16}$$

where R_λ is the responsivity at wavelength λ in volts/watt, V_s the device signal output voltage, H_{sig} the incident signal irradiance in watts/cm^2, and A_D the detector area. H_{sig} corresponding to the blackbody aperture used for Figure 4-31 is 2.78 x 10^{-7} watts/cm^2, and the detector area is A_D = 1.17 x 10^{-5} cm^2 giving

$$R_{2.65\,\mu m} = \frac{30\ mv}{(2.78 \times 10^{-7})(1.17 \times 10^{-5})} = 9 \times 10^9\ volts/watt \tag{4-17}$$

*This is not the longest integration time achievable at this temperature, but one conveniently set by the test set's time mark generator for the particular clock frequency chosen here.

Integration time is, of course, specified by system design and cannot be increased arbitrarily, but this calculation serves to illustrate that the InSb CCIRID is a device with characteristically high voltage responsivity.

The normalized signal-to-noise ratio, or detectivity D*, was roughly estimated for device No. 498-17-B2 under the test conditions of Figure 4-31. The detectivity at the peak wavelength λ_p is calculated from the standard equation for D* using $1/2T_{INT}$ as the bandwidth:

$$D^*\lambda_p = 2\left(\frac{1}{2T_{INT}A_D}\right)^{\frac{1}{2}} \frac{V_s/V_n}{H_{sig}} \qquad (4\text{-}18)$$

where the terms have been previously defined and V_n is the noise voltage. Since signal or dark current variation from element-to-element in the output pulse trains could be repeatably measured on the oscilloscope to better than 2 mv, a first estimate of noise is $V_n \leq 2$ mv. Taking $V_s \cong 30$ mv and substituting in equation 4-18 gives

$$D^*\lambda_p \cong 1.1 \times 10^{11} \text{ cm Hz}^{\frac{1}{2}}/\text{watt}$$

For accurate D* measurements, array 498-17-B2 was shifted to CCD Array Test Set 2. The voltage amplifier shown in Figure 4-18 ($A_V = 10$) was installed in the interface box for the 20-element array. Also a new time mark generator for the 20-element CCIRID which was compatible with Test Set 2 was required, which was designed and fabricated. On Test Set 2, signal and noise were measured for each element using a synchronized sample and hold amplifier. The sampled outputs were then digitized and stored in the HP21-MX memory where signal, noise, and D* calculations were made. Thirty-two lines of signal (blackbody on) and 32 lines of background (blackbody off) data were taken and analyzed by the minicomputer to find averages, variances (noise), and D*.

The results are plotted in Figure 4-32; test conditions are listed in the figure. $D^*\lambda_p$ ranged from 1.5 to 1.13×10^{11} cm $\text{Hz}^{\frac{1}{2}}$/watt. The average

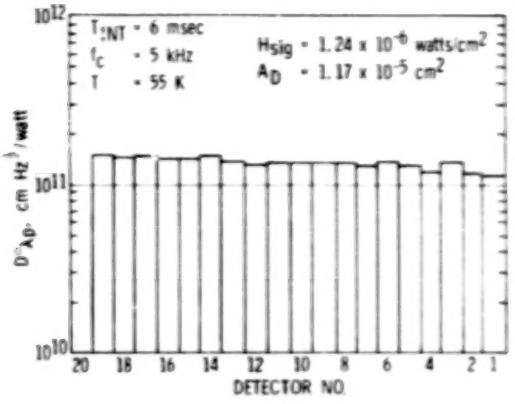


Figure 4-32. - Measured D* of 20-Element CCIRID 498-17-B2 in Multiplexing Mode.

signal was 431 mv and the average noise 13.75 mv (both with 10x voltage gain). The average array $D^*_{\lambda_p}$ is therefore

$$D^*_{\lambda_p} = 1.35 \times 10^{11} \text{ cm Hz}^{\frac{1}{2}}/\text{watt}$$

Optical Input: TDI Mode

Twenty-Element No. 498-17-B2 was also operated with photogate and transfer gate timing changed so as to simulate the time-delay-and-integration mode of operation, thereby demonstrating the feasibility of using InSb CCIRIDs for this on-chip signal processing function. In TDI, and where the CCD array has one bit/detector as in the present case, the condition for TDI is $T_{INT} = T_C$. The period ϕ_T is therefore reduced to T_C and is in phase with ϕ_4, as shown in Figure 4-33. In a TDI sensor, the array is scanned across the scene at a rate such that the image of a given scene element moves along the array in synchronism with the movement of the charge packets in the CCD register. As each charge packet reaches a gate with a detector input port (ϕ_4 in this case) once each clock period, ϕ_T transfers in another packet of detector charge which adds to that already in the register. Repeating this process N times, where N is the number of detectors in TDI, results in an output signal N times larger than each individual detector output. Evaluating a CCD array in the actual system TDI mode necessitates a precision scanning optics system to scan a focused spot along the array.

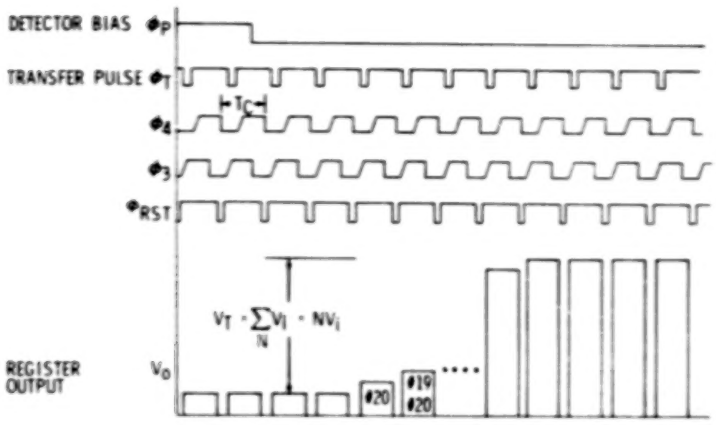


Figure 4-33. - InSb CCIRID Timing Diagram for Demonstration of Time-Delay-and-Integration Mode ($T_{INT} = T_C$).

The TDI mode can be simulated with floodbeam blackbody radiation to show the addition of the individual detector signals using the timing diagram in Figure 4-33. With the array illuminated uniformly with signal radiation, the photogate is switched from an off to an on condition as shown in the top waveform of Figure 4-33. This initiates charge integration by the detectors and transfer of the detector charge into the register each T_C. The resultant output waveform is a pulse train shown at the bottom of Figure 4-33. The first charge packet to reach the output is from detector 20, the second the sum of 20 plus 19, the third the sum of 20 + 19 + 18, and so on, forming an "ascending staircase" pulse train. The output voltage saturates at a voltage $V_T = \sum_N V_i$, where the V_i are the individual detector outputs; if all V_i are equal, then $V_T = NV_i$. The output pulse height remains at V_T as long as ϕ_P is biased on. When ϕ_P is switched off, the opposite process occurs and a "descending staircase" of output pulses results. Twenty-element array 498-17-B2 operating in this manner is presented in Figure 4-34, showing that the TDI addition process is correctly obtained in the InSb CCIRID.

This section has described the test data obtained under this contract for the 20-element CCIRIDs and their witness/evaluation devices. A few devices have been operated over a range of integration times and temperatures, and D* has been measured in the multiplexing mode for one device

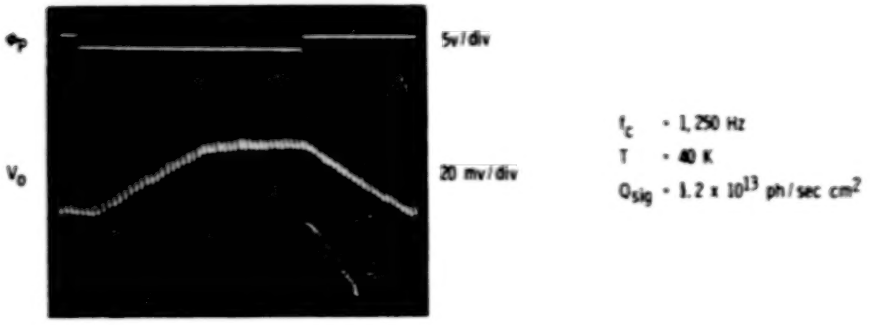


Figure 4-34. - TDI Operation of 20-Element CCIRID 498-17-B2.

under one set of T_{INT}/T conditions. It is evident that much additional test and characterization of the 20-element arrays is required before their complete operational data and performance capabilities are shown. This is further underscored by the fact that the optical mode data were obtained from only one wafer lot. The test results obtained to date, however, have been sufficient to demonstrate the first successful design, fabrication and operation of a fully monolithic InSb infrared CCD array, and to prove the feasibility of this concept.

Some of the factors which influence the current performance of these arrays have been identified, along with means of improvement, and are discussed in the next section.

Section 5

DISCUSSION OF TEST RESULTS

CHARGE TRANSFER EFFICIENCY

Parallel-Edge Surface State Loss

During testing of the two-element InSb CCIRIDs described in Section 3, the observed CTE of the CCDs was assumed to be attributable to the relatively high fast surface state densities measured for the gate oxide witness sample, i.e., midband N_{ss} of 10^{12} cm^{-2}-eV^{-1} (Figure 3-5). Since the majority of the surface states within the channel area are kept filled by the fat zero charge, the inefficiency mechanism to be considered is that due to parallel-edge surface state loss. The "parallel edges" refer to the small areas along the edges of the CCD channel (parallel to the direction of charge transfer) which do not benefit from the fat zero charge. The resulting inefficiency is given by

$$\epsilon_{ss} = \frac{\gamma q k T N_{ss} \ell n(p+1)}{C_{OX} \Delta\psi_{sig}} \qquad (5\text{-}1)$$

where $\gamma = \dfrac{A_S - A_{FZ}}{A_S}$ (5-2)

A_S = total area swept by charge packet (fat zero + signal)

A_{FZ} = area swept by fat zero charge

p = number of phases in CCD

Because the surface potential at the edges of the channel does not increase abruptly to its midchannel maximum value, the area A_{FZ} filled by the FZ charge is smaller than the geometric area of gate length times gate width. When signal charge is transferred down the register, the sloping edges of the well results in the signal charge sweeping a larger area $A_S = A_{FZ} + A_E$, where A_E is an additional area along the channel edges. The factor γ (5-2) represents the ratio A_E/A_S, or the fraction of the total swept area in which

the surface states will contribute to transfer loss. γ is a function of channel width; it can become large for devices with very narrow channels, and is small for wide-channel registers. The 8585 registers are relatively wide (4 mils) for which $\gamma < 0.1$. Using equation (5-1) and temperature and signal charge appropriate to the CTE measurements in Sections 3 and 4, the inefficiency ϵ_{ss} was plotted versus N_{ss} in Figure 5-1. The cross-hatched area in the figure represents a range from the probable upper bound $\gamma = 0.1$ to a lower bound $\gamma = 0.025$.

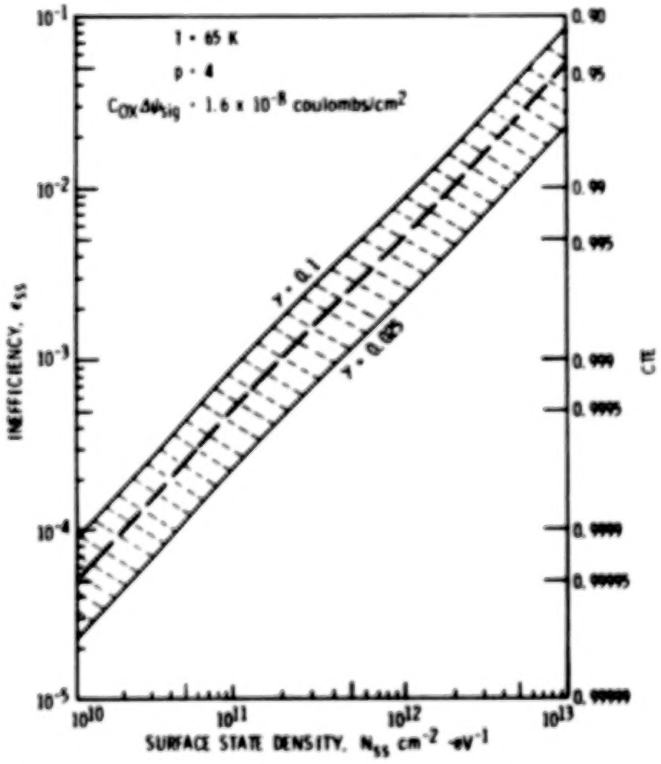


Figure 5-1. - Calculated Inefficiency Range versus N_{ss} for Parallel-Edge Surface State Loss.

For $N_{ss} \cong 10^{12}$ cm^{-2}-eV^{-1}, the measured surface state density for 8585 Lot 4 with gate oxide deposited in the vertical CVD reactor, Figure 5-1 predicts a surface state density-limited CTE in the range of 0.991 to 0.998, in good agreement with measured values (Figures 3-11 and 3-12) about 0.995.

It was, therefore, anticipated that the later lots 8B and 11B, for which quasi-static C-V measurements on their witness wafers indicated a lower midband N_{ss} in the 2 to 5×10^{11} cm^{-2}-eV^{-1} range (Figures 4-6, 4-7, 4-11, and 4-12), would result in somewhat improved CTE. Taking $N_{ss} \cong 3 \times 10^{11}$ cm^{-2}-eV^{-1}, Figure 5-1 shows that CTE would be expected to improve to a range from 0.997 to 0.9993 (an increase which would be clearly detectable in the measurements) if surface state loss were the dominating mechanism. Evidence was simultaneously being obtained which indicated that the N_{ss} calculated from the QS C-V curves was artificially high as well, and that true N_{ss} was much lower than 10^{11} cm^{-2}-eV^{-1}, which offered the promise of even higher CTE.

The measured CTE for the Lot 8B and 11B registers was, surprisingly, not improved from the earlier lot, ranging from 0.992 to 0.9955 (Figures 4-25 through 4-27). Although the model and assumptions leading to Figure 5-1 could certainly lead to errors in quantitative calculation of CTE for a given N_{ss}, a three-to-fivefold decrease in N_{ss} should regardless produce detectable changes. Concurrently with these measurements, evidence was being obtained on SBRC's Two-Dimensional IR Array IR&D Project (in which InSb surface and gate oxide research is being conducted) indicating that the granularity of the SiO_2 layer deposited by low-temperature CVD was influencing the C-V characteristics and complicating N_{ss} analysis. These effects were particularly pronounced for the horizontal-flow CVD reactor used for 8585 Lots 8B and 11B. The question of whether this granularity might be influencing the CTE for the horizontal reactor gate oxide devices was therefore examined.

Transfer Inefficiency Due to Lateral Surface Potential Fluctuation

As was discussed in Section 4, experimental evidence of the presence of lateral nonuniformity of surface potential due to patchiness of the CVD SiO_2 oxide has been obtained. This effect displays itself in C-V diagnostics by a broadening and shallowing of the low-frequency characteristic, which is to be expected from the superposition of a variety of surface regions differing in either oxide fixed charge or permittivity. This results in erroneous

determinations of the surface state density when capacitance methods are used. A C-V characteristic for an InSb MOS sample produced in the horizontal-flow reactor is shown in Figure 5-2, which illustrates this effect. The result of the quasistatic C-V analysis for the data of Figure 5-2 indicates an apparent surface state density in the high 10^{10} $eV^{-1}cm^{-2}$ range. However, inspection of the measured low-frequency C-V curve reveals a symmetrical appearance compared to the ideal which indicates the presence of lateral nonuniformity. This effect masks the true surface state density as has been shown by Castagne, et al[7]. A measurement of the flatband voltage distribution by the method of Chang[8] is shown in Figure 5-3 using the high- and low-frequency data of Figure 5-2. This distribution can also be calculated[7] from a simple parallel array model of equal area 1500Å diameter patches with uniform charge density, but obeying a Gaussian distribution of charge for the noninteracting patches. When the measured distribution of flatband voltages in Figure 5-3 is used to calculate the low-frequency capacitance from the ideal capacitance[8],

$$\overline{C}(V) = \int_{-\infty}^{\infty} C_{IDL}\,(V - V_{FB})\, f\,(V_{FB})\, dV_{FB} \qquad (5\text{-}3)$$

the results totally account for the quasistatic curve in Figure 5-2. Thus surface state densities obtained from capacitance measurements on the LTCVD SiO_2-InSb MOS devices will be higher than the true density due to the spread out of the C-V curves from the nonuniform parallel patch array. This result has been further verified using the frequency test of Chang[8] by high-frequency C-V measurements from 200 Hz to 1 MHz, which show no dispersion in depletion, indicating the lack of surface states.

Laser Mie scattering studies of SiO_2 particulates in CVD reactors[9] have shown that the basic particle nucleation size is between 1000Å and 2000Å. This is further corroborated by the SEM photomicrograph (Figure 5-4) of the horizontal-reactor CVD oxide, which shows a mean particle size of 1500A. Thus, there is little doubt that the pyrolytic CVD process in the horizontal reactor produces a granularity of the same dimension as the surface potential fluctuation length, laterally across the interface.

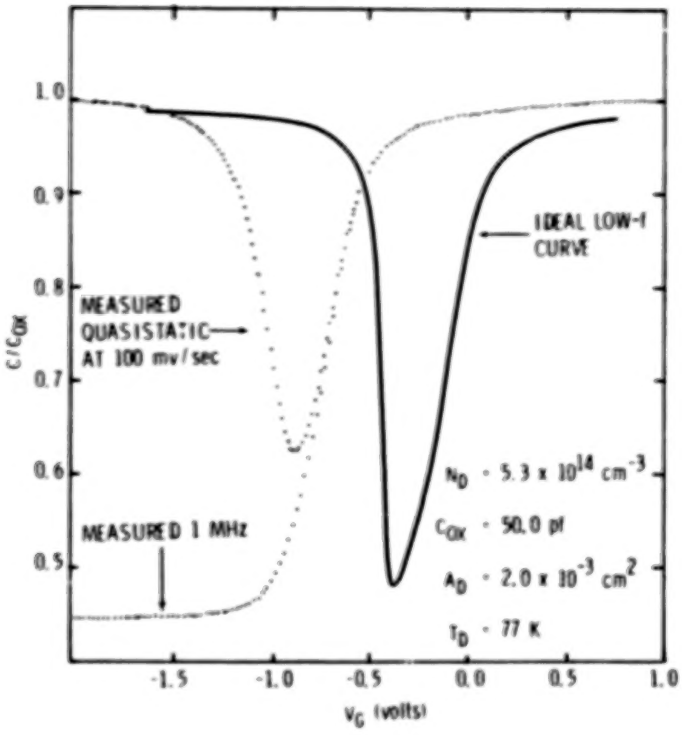


Figure 5-2. - Measured C-V Characteristics of InSb MOS Sample with Gate Oxide Deposited in Horizontal-Flow CVD Reactor.

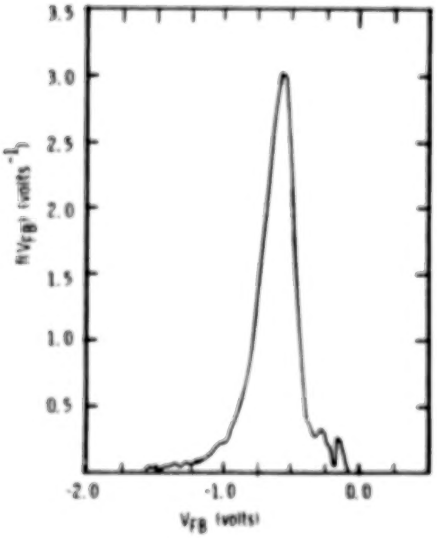


Figure 5-3. - Measured Flatband Voltage Distribution for Sample in Figure 5-2.

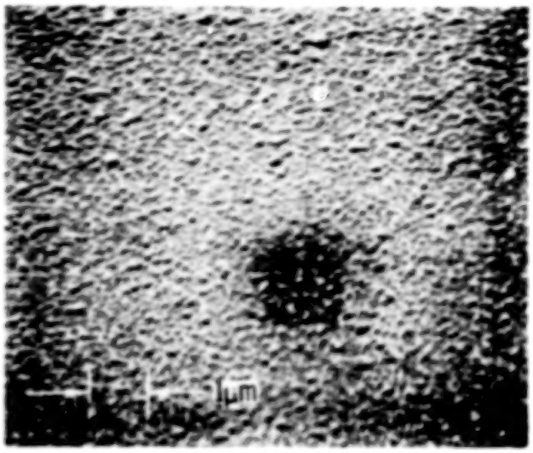


Figure 5-4. - SEM Photo of LTCVD SiO_2 Granularity Resulting from a Horizontal CVD Reactor, Showing Mean Size of 1500Å.

Besides the effect on interface diagnostics, CTE of a CCD also may be influenced by localized variations in surface potential. Charge can be trapped in the small local potential wells and variably emptied depending on lateral electric field amplitudes. Figure 5-5 demonstrates how this variable trapping can cause charge transfer inefficiency. Figure 5-5(a) is a schematic of a 4ϕ CCD and the surface potentials under the gates while transferring a full bucket of charge from ϕ_2 to ϕ_3. As charge flows across the traps, they are filled to a level consistent with a small lateral field and a full bucket. Charge is left behind in the traps, resulting in an incomplete charge transfer. Figure 5-5(b) shows how the charge is recovered in a trailing empty bucket due to the high lateral field tipping or slanting the edge of the trapping wells.

The quantity of charge which is trapped can be calculated to first order by modeling the trap as a well of mean diameter $\bar{d}$ and tipping the trap due to a constant lateral electric field across the trap, as shown in Figure 5-6. The trapped charge difference between having a full well pass under the gate followed by an empty well; i. e., the charge spilled from a single trap, is

$$\Delta Q_{trap} \cong C_{OX} A_t E_y \bar{d}/2 \qquad (5\text{-}4)$$

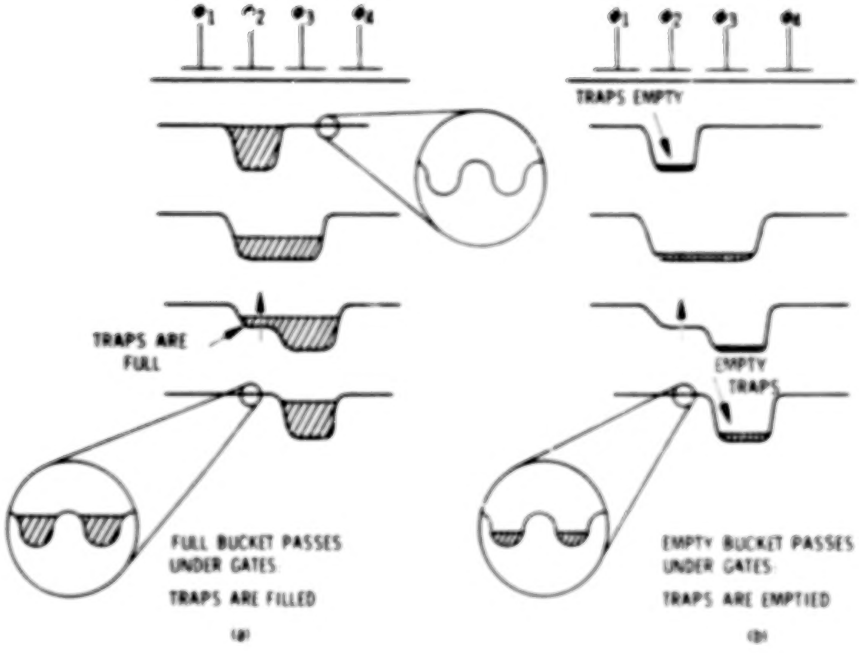


Figure 5-5. - Charge Transfer Inefficiency Mechanism due to Trapping by Localized Surface Potential Variations.

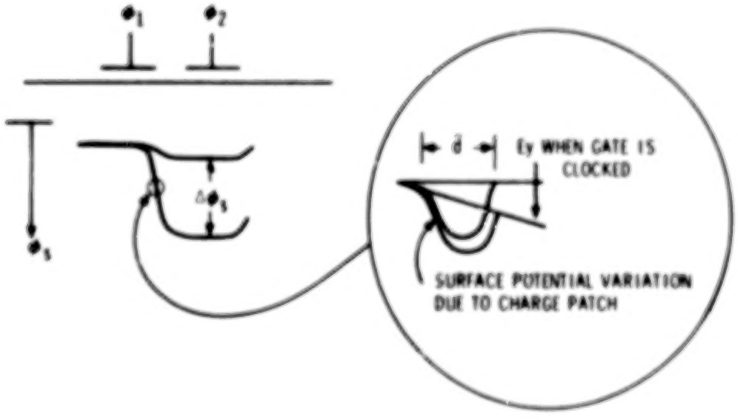


Figure 5-6. - Release of Trapped Charge from Trap in Region of Large Lateral Field.

where C_{OX} is the capacitance per unit area of the gate, A_t the area of the trap and E_y the magnitude of the lateral electric field. The total charge differential trapped under the gate may be found by summing the individual traps:

$$\sum_{\text{over gate}} \Delta Q_{trap} = C_{OX} w \bar{d} \, \Delta \psi_s / 2 \tag{5-5}$$

where w is the gate width and $\Delta \psi_s$ the difference in surface potential between an empty and full bucket. The charge transfer efficiency is then:

$$CTE = 1 - \frac{\sum \Delta Q_{trap}}{Q_{total}} = 1 - \frac{C_{OX} w \bar{d} \, \Delta \psi_s / 2}{C_{OX} w L \, \Delta \psi_s} = 1 - \frac{\bar{d}}{2L} \tag{5-6}$$

where L is the gate length. This result is plotted in Figure 5-7, also including the inefficiency due to fast surface states as a linear sum

$$\epsilon_{total} = \epsilon_{ss} + \frac{\bar{d}}{2L} \tag{5-7}$$

The results of this model predict that a trap diameter (or particle size) of less than 250Å as well as a low surface state density of $\leq 10^{11}$ $cm^{-2}eV^{-1}$ are both needed for a CTE of 0.999. It should be noted that the CTE calculated in Figure 5-7 agrees well with the measured data, i.e., CTE = 0.995 for $\bar{d}$ = 1500Å. A more sophisticated model for charge trapping which takes into account the effects of surface states upon the trap well depth is being developed. The variations from this effect are not expected to be large, but are being investigated for accuracy. Preliminary calculations show that the results are relatively insensitive to patch depths down to the thermal limit

$$\left.\frac{kT}{q}\right|_{77\ K} = 6.6 \text{ mv} \tag{5-8}$$

and thus the simple model for transfer inefficiency can be relied on with small error. The critical parameter is $\bar{d}$, the lateral variation of the surface potential. Since the experimental data from a variety of techniques indicate that the SiO_2 films deposited at ~200°C in the horizontal-flow

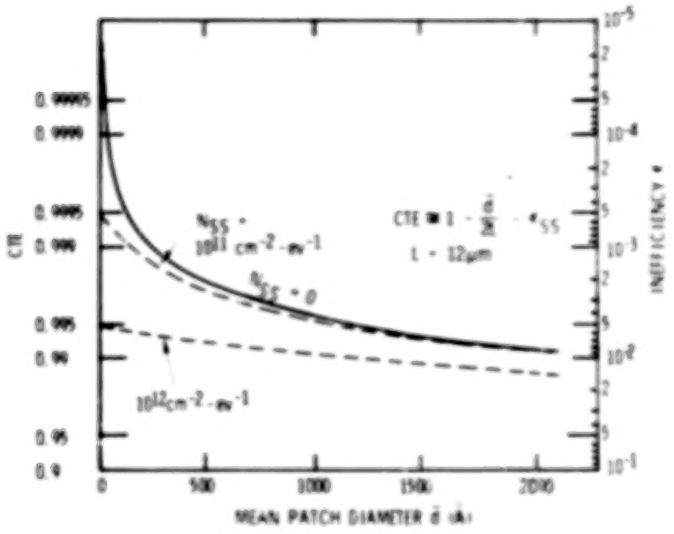


Figure 5-7. - Calculated CTE versus Mean Patch Diameter.

AMS-2600 CVD reactor are characterized by a patchiness with $\bar{d} \cong 1500$Å, we have confidence that the CTE of the 20-element arrays fabricated to date is limited by this effect.

Fortunately, this inefficiency mechanism does not arise from a fundamental limitation to monolithic InSb device performance, but rather from the particular combination of gate oxide deposition technique, reactor geometry, and deposition parameters used so far in the fabrication of the CCIRIDs. Various alternatives are being investigated including other means of depositing SiO_2 and Si_3N_4 at low substrate temperatures, which have been shown in SEM investigations to produce films which are relatively patch-free when compared to the horizontal-flow LTCVD SiO_2. If the low N_{ss} which has been demonstrated can be maintained with simultaneous improvement in the gate oxide morphology, the CTE of the InSb CCDs will approach 0.9999.

LTCVD REACTOR DIFFERENCES

The InSb-LTCVD SiO_2 interface has been the subject of considerable study under an Independent Research and Development project, and the findings have been recently published[4,10]. In this work, conductance measurements did not detect any loss peaks due to interface states on properly prepared devices such as that in Figure 5-2. The sensitivity of the measurements was such that detectable loss in terms of equivalent parallel conductance would have been sufficient to measure surface state densities in excess of 1×10^{10} $eV^{-1}cm^{-2}$. The absence of detectable conductance loss peaks was also found to correlate with the amount of hysteresis in the C-V curves, with devices such as in Figure 5-2 displaying no hysteresis.

It has been determined in this work that the preservation of the thin, native oxide on the InSb surface through a suitable LTCVD process is responsible for the interface properties of devices such as shown in Figure 5-2. The native oxide has been detected both before and after deposition of the LTCVD SiO_2 by Auger Electron Spectroscopy (AES) and X-ray Photoelectron Spectroscopy (XPS). These investigations as well as ellipsometric measurements show the native oxide to be only 10Å to 15Å thick before deposition of the LTCVD SiO_2. The composition of the oxide was determined as In_2O_3, Sb_2O_5 and elemental Sb. After the SiO_2 deposition, no Sb_2O_5 remains, having presumably volatilized. Some elemental Sb remains, however.

Comparing the XPS spectra for the In 3d spin-orbit splitting obtained for samples prepared with the two CVD reactor geometries -- horizontal and vertical -- revealed important differences. The spectra were measured after sputtering through the LTCVD SiO_2 layers, stopping at the point of detection of In for each sample. The two spectra obtained showed a two-component structure with a lower-energy component corresponding to the bulk In (probably from the uneven effect of ion sputtering and the thinness of the native oxide) and a higher energy peak due to In_2O_3, at least in the case of the horizontal reactor sample. The vertical reactor sample, however, clearly displayed a higher oxidation state rather than the In_2O_3 peak. Devices processed

in the vertical reactor show degraded surface state densities, similar in their C-V and G-V characteristics to the data reported by other authors[11, 12]. Our hypothesis is that this is caused in the case of the vertical reactor by a reduction of the thin native oxide by silicon resulting from heterogeneous nucleation of the silane directly on the oxide, thereby disrupting the interface. In the case of the horizontal reactor, as for the sample of Figure 5-2, the silane dissociation reaction is predominantly homogeneous (with SiO_2 particle nucleation size of 1500Å as discussed previously). Thus, the InSb native oxide is protected from reduction by particle nucleation away from the surface in this reactor.

DEVICE OPERATING TEMPERATURE

It was stated in Section 4 that the CCIRIDs from the lots evaluated to date (4, 8B, and 11B) showed best performance in the 60 K to 72 K temperature range, lower than the nominal operating temperature of 77 K. This result is correlated with the storage times measured for these wafer lots, which are shorter than what has been shown previously to be achievable in InSb MOS samples at 77 K[1]. The storage times in the present CCDs have been shown to be limited by dark current from the bulk substrate, rather than generation out of surface states. The higher bulk thermal generation rate may correlate with defects which were discovered in much of the InSb material supplied to us in 1978. These defects are microscopic in nature and were only revealed by a special etchant. Comparative material evaluations have been made possible by growth of InSb layers at SBRC by liquid phase epitaxy (LPE). The LPE technique has been found to be capable of producing very high quality InSb which is both free of these defects and which displays long 77 K MOS storage times. The operating temperature requirements of the 20-element CCIRIDs processed and tested during this program, therefore, are clearly associated with the characteristics of the starting material. Since higher quality InSb has been shown to be possible, InSb CCD arrays with significantly improved temperature characteristics should be achieved in future efforts.

In this section, the relationship of clock frequency and integration time to storage time will be discussed, along with some discussion of the InSb material.

Relationship of CCD Clock Frequency and Storage Time

The storage time (T_S) is related to the dark current density (J_D) by the useful approximation

$$T_S \cong \frac{Q_p(\max)}{J_D} \tag{5-9}$$

where $Q_p(\max)$ is the storage capacity of the well in coulombs/cm^2. Since, in general, the dark current is a function of surface potential $J_D(\psi_s)$, its magnitude changes (usually decreasing) as the well fills with minority carriers. J_D in equation (5-9) is therefore an average over the empty-well to full-well time period.

The dark current at a given temperature establishes a minimum clock frequency for the CCD which increases as the length of the CCD (i.e., number of transfers) increases. Consider a 4ϕ CCD (Figure 5-8) which is transferring a signal charge Q_s in the presence of a small FZ charge Q_{FZ}. The charge $Q_s + Q_{FZ}$ is stored under each gate in the CCD for $T_C/4$ seconds. During this time dark current from an area A_{DK} will add a dark charge Q_D coulombs to the well:

$$Q_D = J_D T_C A_{DK}/4 \tag{5-10}$$

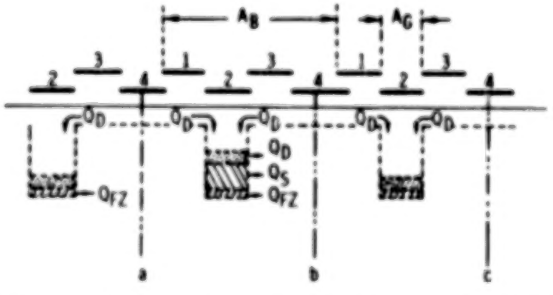


Figure 5-8. - Dark Current in a 4ϕ CCD.

Because all the gates in each bit are not at the same surface potential, it is not straightforward to calculate Q_D exactly. Each gate in the bit contributes its own dark current $I_G = J(\ell_s, Q_p)A_G$ which depends on its surface potential (i.e., whether depleted or inverted), or equivalently the charge stored beneath the gate. We account for this uncertainty by defining an area A_{DK}, which may range from a gate area A_G to as large as the full bit area A_B. If, for example, surface generation dominates the dark current, then $A_{DK} = A_B$. This is shown schematically in Figure 5-8; surface-generated dark current Q_D under the "off" gates surrounding the "on" gate will collect in the storage well. The charge from area a to b will accumulate in one well, from area b to c in the next, etc. Similar to surface generation, if diffusion current from the substrate is the dominant dark current source, the full bit area A_B is the effective dark current area A_{DK}. In the lower limit, if generation out of bulk states in the deep-depleted regions is the principal dark current source, then $A_{DK} = A_G$ since only one gate of a bit is in deep depletion at a given time.

In moving from CCD input to output, a signal charge will encounter N_G gates giving a total accumulated dark charge

$$Q_{DT} = N_G J_D T_C A_{DK}/4 \tag{5-11}$$

or

$$Q_{DT} = N_B J_D T_C A_{DK} \tag{5-12}$$

since $N_G = 4N_B$. But the storage capacity of the CCD is $Q_p(\max)\, A_G$; therefore the accumulated dark charge cannot exceed:

$$N_B J_D T_C A_{DK} \leq Q_p(\max)\, A_G \tag{5-13}$$

Substituting equation (5-9) in (5-13) and solving for T_S gives

$$T_S \leq (N_B T_C)\, (A_{DK}/A_G) \tag{5-14}$$

Note that $N_B T_C$ is the total transfer time of a signal charge from input to output. Equation (5-14) shows that the storage time must be greater than the

transfer time within the numerical factor A_{DK}/A_G which can range from 1 to 4. Writing (5-14) in terms of clock frequency

$$f_c \leq \frac{N_B}{T_S} \frac{A_{DK}}{A_G} \qquad (5\text{-}15)$$

The limit established by equation (5-15), for $N_B = 20$ and $A_{DK}/A_G = 4$, is plotted versus storage time as curve A in Figure 5-9 (left-hand and bottom scales). Two other curves, B and C, for 32- and 100-bit CCDs are also shown for reference. Reading from curve A, for example, if the storage time is 1 msec, the accumulated dark charge will saturate the CCD at $f_c = 80$ kHz. The clock frequency must therefore be higher than the curve A limit by some factor, say 10, to keep the dark charge a small fraction of the CCD capacity.

The measured storage time for the 8585 Lot 8B witness devices was approximately 20 msec at 77 K. Minimum f_c, from curve A, is therefore about 4 kHz at this temperature. Because the storage time varies exponentially with inverse temperature, decreasing the temperature by a few degrees will substantially increase T_S, and consequently lower the minimum clock frequency. The measured temperature dependence of T_S is shown by the top scale in Figure 5-9. At 70 K, T_S has increased to about 100 msec, and at 60 K to 0.7 sec. At 60 K, the clock frequency for saturation has dropped to 100 Hz.

The 20-element CCDs from Lot 8B were found to follow the predicted behavior of Figure 5-9. The points (+) plotted in Figure 5-9 indicate temperature-clock frequency combinations where 20-element devices from Lot 8B were operated with electrical input (photogates off), and where dark charge was maintained as a small fraction of capacity. These points lie on either side of curve D, which is the clock frequency necessary to keep Q_{DT} at 5% of charge capacity. In one test, points E in Figure 5-9, the device temperature was increased from 72 K, where dark charge was $\leq 10\%$, to 80 K, with

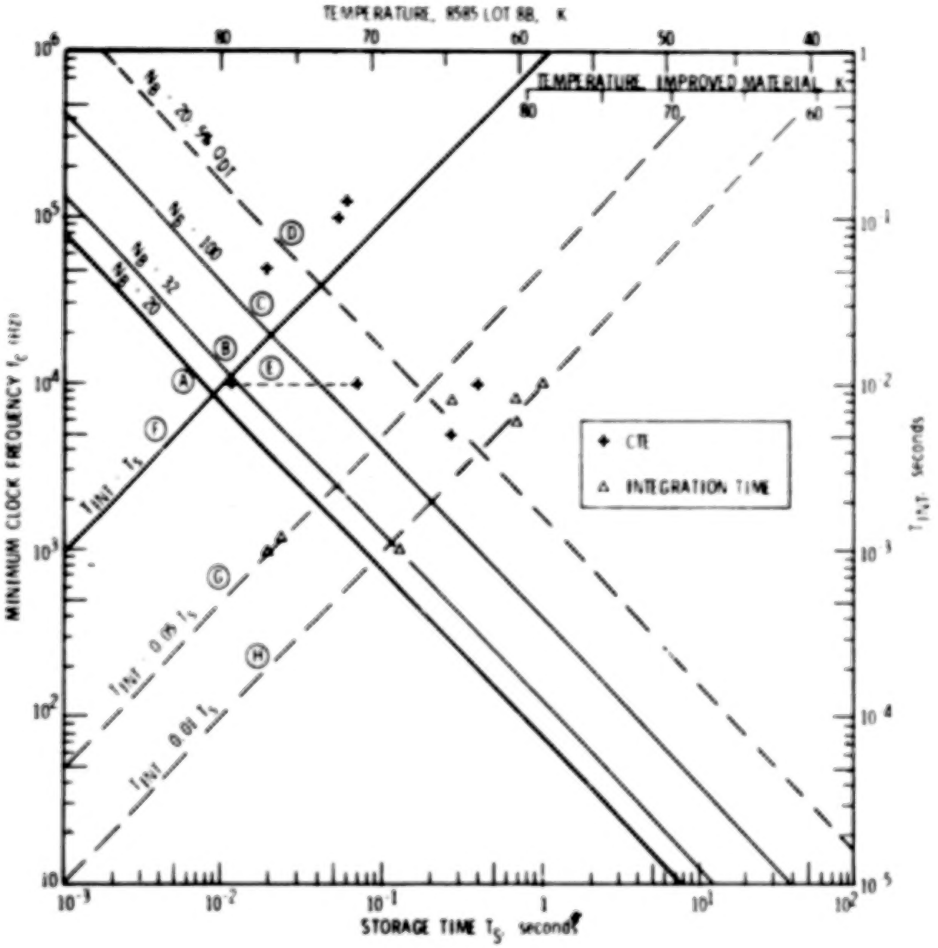


Figure 5-9. - Clock Frequency and Integration Time versus Storage Time.

f_c = 10 kHz. Saturation with dark charge was observed at 79 K, in good agreement with the calculations of Figure 5-9.

Integration Time

The relationship of integration time to storage time is straightforward, i. e. :

$$T_{INT} \leq T_S \tag{5-16}$$

which is plotted as curve F in Figure 5-9 (right-hand and bottom scales). Two other curves, G and H, are also plotted corresponding to 5% and 1% dark charge levels. Triangular data points in the figure correspond to actual temperature-integration time combinations where the 20-element CCIRIDs

were operated in the optical mode with low detector dark charge levels. They are seen to lie between curves G and H as expected.

Comparison of Czochralski-Grown and LPE InSb

Zerbst analysis of the capacitance-time (C-t) responses of MOS samples showing the decreased storage times revealed that they were due to excessive bulk, rather than surface, thermal generation. A change in the quality of the InSb wafers from the Czochralski (CZ) ingots was therefore suspected, although etch pit density, mobility, and other specified parameters of the wafers were meeting specifications. Concurrently, on another program epitaxial InSb layers were being grown by LPE on the CZ wafers which, when impurity concentration and layer morphology were acceptable, provided relevant comparative data. Significant differences in both MOS storage time and leakage currents of implanted Be p-n junctions were observed when fabricated on the LPE InSb layers versus the CZ InSb wafers in hand at that time, both characteristics being superior for the LPE layers.

These electrical differences may correlate with defects observed in the CZ InSb wafers but that were totally absent in the LPE InSb layers. A preferential etchant that reveals defects on the <111>B face of the CZ wafers or epi layers has been developed. A comparison of the results of defect etching a CZ InSb wafer of suspected quality and an epitaxial layer is shown in Figures 5-10 through 5-12. Figures 5-10 and 5-11 show the <111>B face of the CZ InSb wafer after the defect etch, at 2X and 40X magnification, respectively. A large density of etch pits, up to several hundred per square centimeter, is observed. Before performing the defect etch, 20 μm of material was removed from the surface of the CZ InSb wafer with a polish etch to ensure that the pits were not a surface phenomenon, i.e., due to residual polishing damage, the encapsulating material used in shipment, and so forth. The pits revealed by the defect etch do not seem to correlate with dislocations, as when a first set of etch figures is removed with a polish etch and a new set produced with another cycle of defect etching, and second set does not relicate the first. Instead, the predominant sources of the etch figures in the

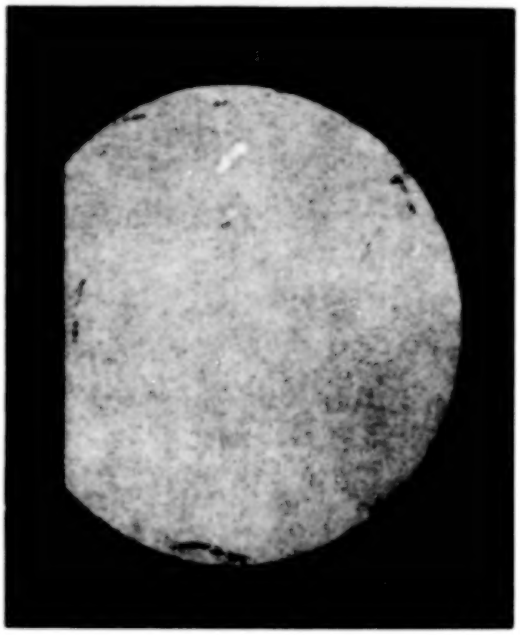


Figure 5-10. - Etch Pits on <111>B Face of CZ InSb Wafer after Etching to Reveal Defects (2X).

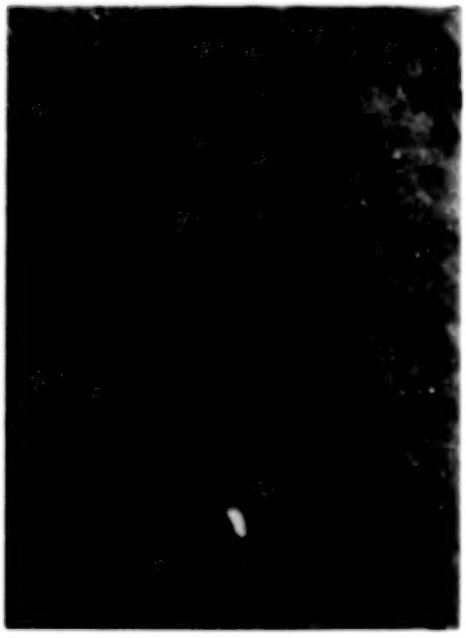


Figure 5-11. - Etch Pits on CZ InSb Wafer at Higher Magnification (40X).

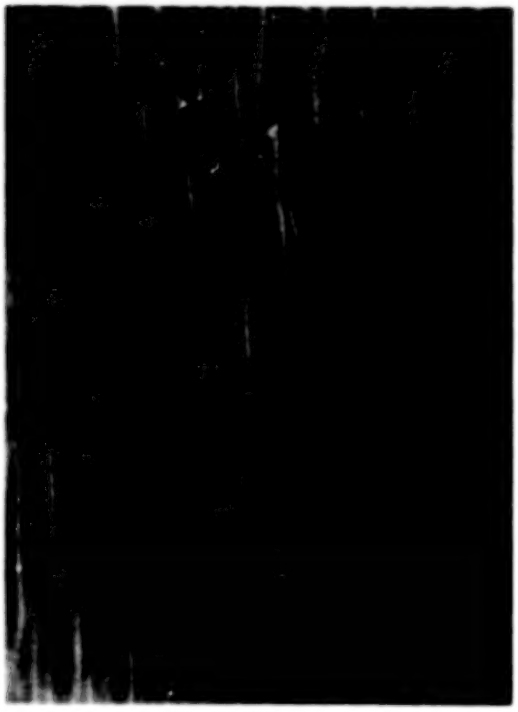


Figure 5-12. - <111>B Face of LPE InSb Layer after Defect Etching (Phase Contrast Photomicrograph) (40X).

CZ material are thought to be chemical complexes, probably oxides, randomly included throughout the crystal. The low storage time of the MOS capacitors on the CZ InSb suggests that these complexes may be electrically active. The density of these defects varies from ingot to ingot, and Figures 5-10 and 5-11 probably represent a worst case. Pits revealed by the defect etch also can be due to other sources such as mechanical damage. For example, the lines of pits near the edge of the wafer visible in Figure 5-10 are from handling work damage which occurred when it underwent the etch process.

Performing the same defect etch on wafers received recently indicates that CZ ingots can be grown considerably more defect-free than that illustrated in Figure 5-10. A CZ wafer from a second InSb source, subjected to the same defect etch, had fewer pits compared to Figures 5-10 and 5-11 but was not free of the defects. A new Czochralski puller set up by the first

InSb supplier has recently produced material with significantly lower defect count than that illustrated in Figures 5-10 and 5-11.

After etching the LPE InSb layer in the B-face defect etch, no pits or etch figures were developed over the majority of the wafer area, indicating the total absence of the defects or complexes that were found in the CZ InSb. Figure 5-12 shows the <111>B face of the LPE InSb layer after defect etching. The magnification in the photomicrograph of Figure 5-12 is the same as that of Figure 5-11, and phase contrast was used to enhance the surface morphology.

MOS samples fabricated on low impurity concentration LPE InSb layers showed long storage times characteristic of good substrate material. Figure 5-13 shows a C-t characteristic for a capacitor processed on the higher quality material, following application of a voltage step. The 77 K storage time is seen to be about 1.5 seconds. With improved material leading to storage times of this order, a broader range in clock frequency and integration time will result. This is shown in Figure 5-9 by a second temperature scale for the improved material at the top right-hand of the figure. At 77 K, the 20-element CCIRID will not be dark current saturated until the clock frequency is reduced to 50 Hz, a clock rate orders of magnitude lower than most anticipated systems require.

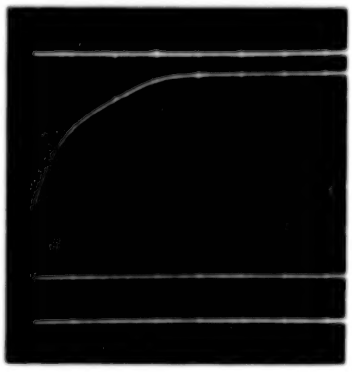


Figure 5-13. – MOS Storage Time at 77 K for LPE InSb Layer.

IMPROVEMENTS IN PHOTOGATE YIELD

One fabrication process change required for increased yields is to reduce the number of photogate-to-substrate shorts which were observed in the 8585 linear imagers processed in this program. Since all the photogate elements of an imager are in parallel, one short in the array renders it inoperable. Examination of completed arrays utilizing scanning electron microscopy showed that these shorts occurred in the contact windows to the photogates, not in the optically-active areas themselves. In the process sequence that was used*, the photogates were very thin (0.0075 μm) evaporated titanium, on the same level as (but not electrically connected to) the buried metal gates (see Figure 2-5). Both the photogates and buried metal were subsequently insulated with a 2000A thick SiO_2 buried metal insulator. Contact windows were then etched through the buried metal insulator to the photogates to allow the next metal layer (surface metal) to contact them. During this contact window etching process, pinholes were exposed allowing etching of the underlying SiO_2 layers to the InSb substrate surface, causing the shorts.

The photomicrographs in Figure 5-14 show these pinholes which were exposed and the photogate-to-substrate shorts created. The mechanism by which this pinholing occurred is not clearly understood, since the surface of the oxide under the photogates is identical to the oxide under the contact. Pinholes in the gate oxide, if they exist, should be visible throughout the channel region, and they were not detected there. Having identified the origin of the shorts, a change in process sequence will alleviate the photogate contact window pinholes in future 8585 wafer lots. Also, the process and mask design for the next-generation InSb CCIRID chip will be such as to preclude this problem entirely by having the photogates and their bias bus bar on the same metal level, thus eliminating the contact cut step.

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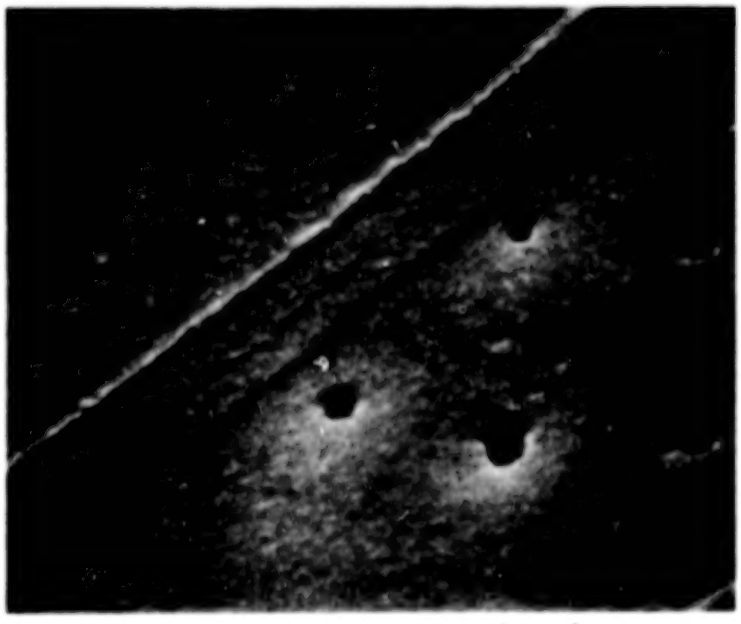
*SBRC is working on development of an antireflective, conductive gate structure on IR&D for future use as optimized photogates with improved transmittance characteristics.

TRANSPARENT GATE AND CONTACT WINDOW



PINHOLES IN CONTACT WINDOW

Figure 5-14. - 8585 InSb CCIRID Transparent Gate Structure.

Section 6

APPLICATIONS FOR MONOLITHIC InSb CCD ARRAYS

This section describes part of a continuing survey of future instruments and sensor systems in which potential applications exist for the monolithic InSb CCIRID technology that is being developed. Space applications for monolithic InSb arrays fall into several areas where the construction of the device offers operational and reliability advantages over more conventional discrete or hybrid array technologies. Described in more detail in the following are three of these areas: earth resources applications; meteorological satellite applications; and geological applications.

EARTH RESOURCES APPLICATIONS

The Earth Observatory Satellite (EOS) Mission involves remote sensing from space and transmitting, processing, and delivering earth observational data by the most cost-effective methods to the user community concerned with earth resources management. The user community is represented by: NASA - sponsored principal investigators and their associates; other U. S. federal, state, and local government agencies; foreign government agencies (some of whom have their own earth stations); universities; and private industry around the world. Satisfying this diverse user community is a task that NASA has undertaken and accomplished since the first LANDSAT spacecraft with a four-band multispectral scanner (MSS) and a three-band return beam vidicon was launched in 1972. The launch in January 1975 of the LANDSAT-2 spacecraft with its multispectral scanners provided a system that currently generates updated earth resources data in a geographical area every nine days.

The experience with the two in-orbit multispectral scanners has been the basis for evolving the requirements for the Thematic Mapper (TM), the primary instrument for the EOS or advanced LANDSAT System which is currently being built by the Hughes Aircraft Company. The TM will be

installed in the multi-mission modular spacecraft and launched by the Delta B910 or space shuttle in late 1981.

The specified ground resolution of the TM is 30 meters for the reflective infrared and visible bands, as opposed to 80 meters for the currently in-orbit multispectral scanners; however, improved ground resolution to 15 meters is currently being studied in connection with an upgraded TM to be flown on LANDSAT D' in 1983.

The current TM employs among others two arrays each containing 16 staggered InSb elements, one covering the 1.55- to 1.75-μm band and the other in the 2.08- to 2.35-μm band. These bands are used for agriculture and geological resource monitoring, respectively. A scan mirror is used to scan these arrays across the ground track such that a swath 185 km wide is generated. The scan rate used to ensure contiguity of consecutive swaths produces a dwell time of less than 10 μsec, a value much too short to use photoconductive PbS which would otherwise be suitable for these spectral ranges. The 32 InSb elements together with their preamplifier input stages used in the TM are cooled to a temperature of about 80 K by a passive radiative cooler.

Improvements to the present TM design may include replacement of the two conventional or discrete element InSb arrays with two monolithic InSb time-delay-and-integration (TDI) CCIRID arrays (32 cross scan, 16 TDI) which will give double the present resolution (15 meters) and approximately the same signal-to-noise ratio. To maintain contiguity of the fields of view in the TDI direction, the detector/TDI CCD rows would be staggered. This can be accommodated by the use of a fiber optic relay between the focal plane and CCD array chip, allowing full utilization of the TM focal plane as presently configured.

METEOROLOGICAL SATELLITE APPLICATIONS

Meteorological observations from space include infrared and visible imaging primarily to observe cloud motion, night or day. Thermal measurements of cloud tops to obtain temperatures allow the determination of wind velocity as a function of altitude if the lapse rate is assumed.

Temperature sounding is a method by means of which the temperature profile in the atmosphere can be determined remotely. To do this, we must observe the radiation emitted by an atmospheric constituent whose vertical distribution (concentration) and radiating properties are known so that the transmittance (τ) and the slope of transmittance with pressure ($d\tau/dP$) are calculable. This requires that the radiation emanate from a gas which has a known, stable concentration and that this radiation be separable from all other sources, gaseous or aerosol. The gases usable for temperature profiling are CO_2 in the 2325 cm^{-1} (4.3-μm) or the 668 cm^{-1} (15-μm) band and O_2 in the 60-GHz microwave band. CO_2 is assumed to be essentially uniformly distributed throughout the atmosphere. The technique is to observe radiation emitted within several spectral regions in the CO_2 absorption bands - each of which has a different transmittance. The effect of this is to cause the observed radiances to originate from a different altitude. Extraction of atmospheric temperatures from radiances is not an exact process since the radiances are not independent. The procedure is to use a first "guess" for the temperature profile based on the latest forecast or from climatology. Then by using regression analysis of the differences between the first guess and the observed radiances a better answer can be obtained.

Temperature Sounding from Synchronous orbit is currently being planned by NASA using a modified version of the Visible Infrared Spin-Scan Radiometer (VISSR) built by SBRC. The sensor, known as the VISSR Atmospheric Sounder (VAS) uses several channels in each of the 4.3-μm and 15-μm CO_2 bands. Sounding performance is limited, however, by the scan efficiency which is low owing to the fact that the earth is viewed for about 5% of the spin period at

synchronous orbit. This necessitates dwell spinning for many revolutions to build up the signal-to-noise level.

Future improvements to this design include upgrading of the focal plane through the use of monolithic InSb and HgCdTe TDI CCD arrays for the 4.3-μm and 15-μm bands, respectively. Arrays of up to 40 elements in each band can be accommodated which will give a signal-to-noise improvement of about six over the present VAS.

Future sounder developments also include consideration of line-of-sight stabilized sensors from synchronous orbit. The increased scan efficiency of this type of sensor as compared with the spin-stabilized VAS will give improved performance. Use of CCD area arrays in this application will simplify the scan, and improve performance further. Spatial registration of fields of view in the various spectral regions is important to sounding (registration to within 1% of footprint area is a commonly used requirement). This becomes possible with a monolithic array in which the position of elements is controlled with photoetch masks.

GEOLOGICAL APPLICATIONS

A current development at the Jet Propulsion Laboratory (JPL) is the Shuttle Multispectral Infrared Reflectance Radiometer (SMIRR). The first experiment will measure from an aircraft the solar reflectance spectra of surface minerals between 0.6 μm and 2.25 μm. The second experiment, known as "Son of SMIRR," will be flown from the Space Shuttle. It will use a two-dimensional array of upwards of 1000 elements. The monolithic InSb CCD array technology would work well in this application. Cooling will be provided by either a liquid cryogen or a cryogenic refrigerator.

Section 7

SUMMARY

Monolithic infrared CCD linear imaging arrays were successfully fabricated in InSb, and IR detection and readout with the arrays demonstrated, in this contract. Twenty MOS detector elements were integrated on the same chip with a 4ϕ, surface-channel InSb CCD to produce a charge-coupled infrared imaging device (CCIRID). The development of this technology allows several signal processing functions to be accomplished on the detector array chip instead of off-focal-plane as in current systems. The InSb CCDs can be used for on-chip multiplexing of the detector outputs, or to provide time-delay-and-integration (TDI) for signal/noise enhancement in scanning systems.

The CCD process developed for InSb includes a capability for p-n junctions, which are used in the present device for fat zero (FZ) input and charge output; InSb MOSFETs have also been fabricated. The availability of these components will allow critical output circuit elements to be incorporated on-chip in the next InSb CCIRID design along with the possibility of detector ac coupling, background subtraction, and antiblooming circuits in future arrays. The fabrication process is suitable for large area arrays, and design and fabrication of an area array should be undertaken as one of the next tasks in this development.

The CTE of the InSb CCDs fabricated during this program was measured to be 0.995. The 20-element CCIRIDs evaluated were produced in two 8585 wafer fabrication lots (Nos. 8B and 11B), in which the LTCVD SiO_2 gate oxide was deposited by means of a horizontal-flow configuration CVD reactor. True surface state density of InSb MOS devices produced in this reactor has been shown to be very low ($\sim 10^{10}$ cm^{-2}-eV^{-1}), and CTE should be correspondingly high, 0.9995 or better. The CTE of this device group was found, in fact, to be not limited by surface states but rather by lateral nonuniformity in

surface potential arising from the microscopic granularity of the LTCVD SiO_2 oxide layer. This limitation is not fundamental to InSb CCDs or CCDs in general, and alternate SiO_2 deposition techniques are being pursued in an SBRC Independent Research and Development program to greatly reduce or entirely eliminate the oxide granularity, while preserving the low N_{ss} values that we have successfully demonstrated on InSb.

In addition to low surface state density, other characteristics of the LTCVD SiO_2-InSb MOS system are very favorable for CCD arrays, such as the near-zero flatband voltage. Fixed charge density in the gate oxide is approximately 10^{11} (positive) charges/cm^2 or less, comparable to typical silicon CCD devices. This results in low drive voltage requirements, as well as compatibility with p-n junctions on chip: i.e., the lightly-doped side of the junctions are neither strongly accumulated nor inverted by a large oxide fixed charge.

Charge integration in the photogates, transfer into the register, and serial readout of the 20 detector signals was demonstrated for the InSb linear CCIRIDs. Because of its inherent flexibility, application of the InSb CCIRID concept in future IR sensors will offer many advantages. The CCD clock frequency, and thus the array readout rate, is variable over a wide range to suit system needs. In the first device tests reported here, the 20-element CCIRID clock frequency ranged from 1 to 200 kHz. With storage time improvements gained through improved InSb material quality (which has been demonstrated), the 20-element CCIRID will have a 77 K operational clock frequency range from a few hundred Hertz to over 1 MHz. Since the CCD registers are 4ϕ, they can also be clocked in reverse allowing the design of bidirectional scanning arrays. The separation of detection and multiplexing functions in the InSb CCIRID allows the integration time to be varied independently of readout rate from $T_{INT} = f_c^{-1}$, the TDI mode, to $T_{INT} \gg Nf_c^{-1}$, where the N detectors in the array are read out during a small fraction of the integration time. Both operational modes were demonstrated during this program. Integration times of several hundred milliseconds at 77 K are

feasible for low background photon flux levels. If applications require it, even longer integration times can be obtained with lower operating temperatures. Storage times have been measured as a function of temperature and increase to $>10^2$ sec at 50 K and $>10^3$ sec for lower temperatures.

The output voltage magnitude (and therefore responsivity) of the present devices is reduced by the interim use of discrete silicon MOSFETs in the output circuit rather than on-chip transistors. The sum of output diode, MOSFET input, bonding pad, and stray capacitances on the output node is about 6 pf, which results in a full-well output voltage of 60 mv. Nearly an order of magnitude improvement will be obtained with critical elements in the output circuit integrated monolithically on the InSb chip. The potential for on-chip transistors has been established by separately fabricating InSb MOSFETs, utilizing the Be-implant procedure to produce planar source and drain and LTCVD SiO_2 for the gate oxide. The InSb FETs are p-channel enhancement-mode devices and show promise for several on-chip applications.

The D^* was measured for one 20-element InSb CCIRID operating in the multiplexing mode and was greater than 10^{11} cm-Hz$^{\frac{1}{2}}$-watt^{-1} at low background and for the particular clock and integration time conditions of the test. With improvements in both the transparent photogate process (increasing the present transmittance from ~ 30% to > 70%) and the output circuit, array $D^* > 10^{12}$ cm-Hz$^{\frac{1}{2}}$-watt^{-1} is predicted for backgrounds less than 10^{14} ph/sec-cm^2. This is the single-element D^* and a further $\sqrt{N}$ improvement should be obtained with TDI.

Two 20-element InSb CCIRIDs fabricated in the program were delivered to NASA Langley Research Center for further evaluation, device Nos. 498-17-A3 and 498-17-F4.

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Final Report

16. Abstract

This report describes the design and fabrication of the 8585 InSb Charge Coupled Infrared Imaging Device (CCIRID) chip, on which a 20-element linear imager is the principal device, and the electrical and optical characteristics of the experimental devices that were determined under this contract. The report is organized as follows: device design and fabrication, including discussion of the InSb material characteristics; the design and description of the 8585 chip; the fabrication process; and mask and process modifications that were implemented in the program. Test results for the two-element InSb CCIRID on the 8585 chip are discussed, which was the first device produced. Included are: evaluation of the gate oxide characteristics; development of the surface potential diagram; discussion of the CCIRID channel stopping approach; and operation of the two-element device. A similar discussion of the test results for the 20-element CCIRID, including gate oxide characteristics, test equipment configuration, measurement of charge transfer efficiency, and optical mode operation is presented. A discussion of test results examines some of the factors that have been identified which influence the current performance of these arrays is presented, along with means of improvement.

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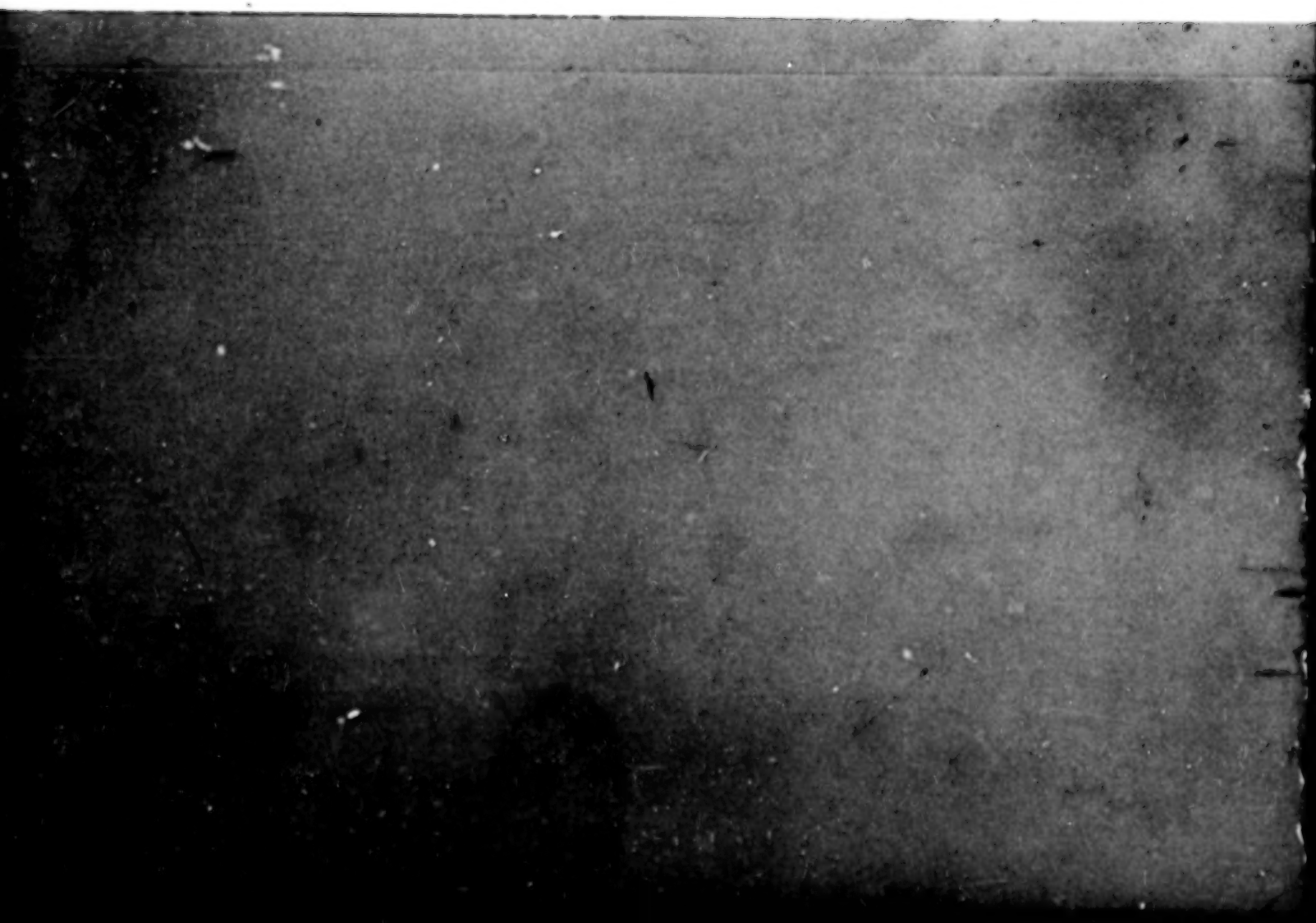

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